```
Successfully removed tdl files
Successfully started file /tmp/advantest/_default/hardware.tdl
********************************************************************************
****
* DIAGNOSIS VERSION     R2.06    (for    viewpoint    R8.05    or    later)
*
* SYSTEM NAME           T6672
*
* DIAGNOSIS STARTED AT 2022/04/07 13:28:47
*
********************************************************************************
****
 ----- SYSTEM CONFIGURATION INFORMATION ------------------------------------
--
 PIN CONFIGURATION
  MAINFRAME             :    1 -  512
  TH1    [CTD         ] :    1 -  512
 DPU CONFIGURATION
  DPS CH       [TH1]    :  1 - 32
  UDC CH       [TH1]    :  1 -  4
  MDC CH       [TH1]    :  1 - 32
  DPS HS MODE           : OFF
  DPS PSRR              : OFF
 LINE FREQUENCY         : 50Hz
 DMM MODEL              : R6581T
 SQPG CONFIGURATION
  MAX VGC               : 4MW
  MAX CTB               : 64MW
  MAX TTB               : 16MW
 OPTIONS CONFIGURATIONS : HRS OFF  SCPG ON   ALPG ON   MIXED ON  MIXED2 OFF
  OPTION PG
   MAX SCPG             : 4Gbit
   MAX ALPG             : 1KW
   MAX PM               : 4MW
   PDS                  :    1 -  512
   MDS         [TH1]    :    1 -  512
```

```
   FMUX        [TH1]    :    1 -  512
  MIXED OPTION [TH1]    : BASICS[CAL EM CM1] DCAP
                        : AFG    1 2 3 4
                        : AFD    1 2 3 4
                        : VFG    1 2
                        : VFD    1 2
 HI-FIX TYPE   [TH1]    : 512B[512+Mixed+VFD/VFG+ASPE]
 ------------------------------------------------------------------------
---
 ----- DIAGNOSIS INFORMATION ---------------------------------------------
--
 DIAGNOSIS MODE         : NORMAL
 DIAGNOSIS TEST NUMBER  :     -1 -     -1
 DIAGNOSIS SPEC.        : 100.0
 DIAGNOSIS REPEAT COUNT : 1
 DIAGNOSIS PIN INFORMATION
  MAINFRAME             :    1 -  512
  TH1                   :    1 -  512
 DIAGNOSIS DPU INFORMATION
  DPS CH       [TH1]    :  1 - 32
  UDC CH       [TH1]    :  1 -  4
  MDC CH       [TH1]    :  1 - 32
 DIAGNOSIS OPTIONS INFORMATION
  OPTION PG
   PDS                  :    1 -  512
   MDS         [TH1]    :    1 -  512
   FMUX        [TH1]    :    1 -  512
  MIXED OPTION [TH1]    : BASICS[CAL EM CM1] DCAP
                        : AFG    1 2 3 4
                        : AFD    1 2 3 4
                        : VFG    1 2
                        : VFD    1 2
 ------------------------------------------------------------------------
---
TEST 141000 TH1 PIN/CW/PCON PB CONNECTION CHECK
    ERNO CH LOAD  S_RNG S/CLP_DATA  M_RNG MEAS_DATA   IDEAL_DATA  ERROR_DATA
```

```
LIMIT_DATA  MXMN GO/NOGO
      30 31 100KR  80uA  0.0000e+00     8V -1.9978e-08  0.0000e+00 -1.9978e-
08  1.7749e-08     0 ____AA_
      40 31  10KR 800uA  0.0000e+00     8V -1.9833e-07  0.0000e+00 -1.9833e-
07  1.7751e-07     0 ____AA_
      50 31   1KR   8mA  0.0000e+00     8V -1.9612e-06  0.0000e+00 -1.9612e-
06  1.7749e-06     0 ____AA_
    CHECK COUNT =     3187    FAIL COUNT =        3
TEST  141000  RESULT  ====================================  13:36:00  ==>
FAIL***
TEST 144500 TH1 DRIVER/COMPARETER TR/TF CHECK
INIT VIL OFFSET     PIN=  173 REG= 0X092A LIMIT=   0.014 ,  -0.014 MEAS=  -
0.015 *** FAIL
0101730172.DR: 173 CP: 172 UPPER=1.861 LOWER=0.239 HCP TR=29.188 *** FAIL
0201730172.DR: 173 CP: 172 UPPER=1.861 LOWER=0.239 HCP TF=30.906 *** FAIL
0301730172.DR: 173 CP: 172 UPPER=1.861 LOWER=0.239 LCP TR=28.375 *** FAIL
0401730172.DR: 173 CP: 172 UPPER=1.861 LOWER=0.239 LCP TF=31.937 *** FAIL
0101860191.DR: 186 CP: 191 UPPER=1.861 LOWER=0.239 HCP TR=2.281 *** FAIL
0201860191.DR: 186 CP: 191 UPPER=1.861 LOWER=0.239 HCP TF=2.313 *** FAIL
0301860191.DR: 186 CP: 191 UPPER=1.861 LOWER=0.239 LCP TR=2.188 *** FAIL
0401860191.DR: 186 CP: 191 UPPER=1.861 LOWER=0.239 LCP TF=2.188 *** FAIL
0101910186.DR: 191 CP: 186 UPPER=1.861 LOWER=0.239 HCP TR=2.156 *** FAIL
0201910186.DR: 191 CP: 186 UPPER=1.861 LOWER=0.239 HCP TF=2.125 *** FAIL
0301910186.DR: 191 CP: 186 UPPER=1.861 LOWER=0.239 LCP TR=2.063 *** FAIL
0401910186.DR: 191 CP: 186 UPPER=1.861 LOWER=0.239 LCP TF=2.188 *** FAIL
0104090416.DR: 409 CP: 416 UPPER=1.861 LOWER=0.239 HCP TR=2.094 *** FAIL
0204090416.DR: 409 CP: 416 UPPER=1.861 LOWER=0.239 HCP TF=2.531 *** FAIL
0304090416.DR: 409 CP: 416 UPPER=1.861 LOWER=0.239 LCP TR=3.000 *** FAIL
0404090416.DR: 409 CP: 416 UPPER=1.861 LOWER=0.239 LCP TF=3.062 *** FAIL
0104160409.DR: 416 CP: 409 UPPER=1.861 LOWER=0.239 HCP TR=3.156 *** FAIL
0204160409.DR: 416 CP: 409 UPPER=1.861 LOWER=0.239 HCP TF=3.187 *** FAIL
0304160409.DR: 416 CP: 409 UPPER=1.861 LOWER=0.239 LCP TR=2.688 *** FAIL
0404160409.DR: 416 CP: 409 UPPER=1.861 LOWER=0.239 LCP TF=2.625 *** FAIL
0104670470.DR: 467 CP: 470 UPPER=1.861 LOWER=0.239 HCP TR=5.688 *** FAIL
0204670470.DR: 467 CP: 470 UPPER=1.861 LOWER=0.239 HCP TF=5.750 *** FAIL
0304670470.DR: 467 CP: 470 UPPER=1.861 LOWER=0.239 LCP TR=5.719 *** FAIL
```

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0404670470.DR: 467 CP: 470 UPPER=1.861 LOWER=0.239 LCP TF=5.750 *** FAIL
0104700467.DR: 470 CP: 467 UPPER=1.861 LOWER=0.239 HCP TR=5.750 *** FAIL
0204700467.DR: 470 CP: 467 UPPER=1.861 LOWER=0.239 HCP TF=5.750 *** FAIL
0304700467.DR: 470 CP: 467 UPPER=1.861 LOWER=0.239 LCP TR=5.719 *** FAIL
0404700467.DR: 470 CP: 467 UPPER=1.861 LOWER=0.239 LCP TF=5.719 *** FAIL
THU         SLOT 13           BGR-024908     (ACA) IS BAD
FPU1        SLOT 14           BMR-025625     (CBA) IS RELATED
THU         SLOT 22           BGR-024908     (ACA) IS BAD
FPU2        SLOT 13           BMR-025625     (CBA) IS RELATED
FPU2        SLOT 15           BMR-025625     (CBA) IS RELATED
    CHECK COUNT =    14336    FAIL COUNT =       29
TEST   144500   RESULT   ==================================   13:41:21   ==>
FAIL***
TEST 102543 DPU  STN1  MDC   ISVM IS       INITIALIZE
    ERNO CH LOAD  S_RNG S/CLP_DATA  M_RNG MEAS_DATA   IDEAL_DATA  ERROR_DATA
LIMIT_DATA  MXMN GO/NOGO
      30 31 100KR  80uA  0.0000e+00    8V -1.9768e-08  0.0000e+00 -1.9768e-
08  1.7749e-08    0 ____AA_
      40 31  10KR 800uA  0.0000e+00    8V -1.9753e-07  0.0000e+00 -1.9753e-
07  1.7751e-07    0 ____AA_
      50 31   1KR   8mA  0.0000e+00    8V -1.9652e-06  0.0000e+00 -1.9652e-
06  1.7749e-06    0 ____AA_
    CHECK COUNT =      640    FAIL COUNT =        3
TEST   102543   RESULT   ==================================   13:45:48   ==>
FAIL***
TEST 103733 DPU  STN1  DPS   VSIM IM       ACCURACY CHECK
    ERNO CH LOAD  S_RNG S/CLP_DATA  M_RNG MEAS_DATA   IDEAL_DATA  ERROR_DATA
LIMIT_DATA  MXMN GO/NOGO
      21  9   1MR    8V  8.0000e+00   5uA -1.8000e-08  0.0000e+00 -1.8000e-
08  1.7000e-08    3 ____AA_
      22  9   1MR    8V -6.0000e+00   5uA  2.3000e-08  0.0000e+00  2.3000e-
08  1.3002e-08    3 ____AA_
      22 10   1MR    8V -6.0000e+00   5uA  2.2000e-08  1.0000e-09  2.1000e-
08  1.3001e-08    3 ____AA_
      22 11   1MR    8V -6.0000e+00   5uA  1.9000e-08  2.0000e-09  1.7000e-
08  1.3001e-08    3 ____AA_
```

```
      22 12    1MR     8V -6.0000e+00    5uA  2.1000e-08  0.0000e+00  2.1000e-
08  1.3001e-08     2 ____AA_
      22 13    1MR     8V -6.0000e+00    5uA  2.2000e-08  2.0000e-09  2.0000e-
08  1.3002e-08     3 ____AA_
      22 14    1MR     8V -6.0000e+00    5uA  2.1000e-08  2.0000e-09  1.9000e-
08  1.3000e-08     3 ____AA_
      22 15    1MR     8V -6.0000e+00    5uA  1.9000e-08  0.0000e+00  1.9000e-
08  1.3001e-08     3 ____AA_
      22 16    1MR     8V -6.0000e+00    5uA  1.7000e-08  0.0000e+00  1.7000e-
08  1.3002e-08     3 ____AA_
      22 17    1MR     8V -6.0000e+00    5uA  1.8000e-08  1.0000e-09  1.7000e-
08  1.3000e-08     4 ____AA_
      22 18    1MR     8V -6.0000e+00    5uA  1.5000e-08  0.0000e+00  1.5000e-
08  1.3000e-08     3 ____AA_
      22 19    1MR     8V -6.0000e+00    5uA  1.9000e-08  1.0000e-09  1.8000e-
08  1.3000e-08     3 ____AA_
      22 20    1MR     8V -6.0000e+00    5uA  1.8000e-08  0.0000e+00  1.8000e-
08  1.3001e-08     4 ____AA_
      22 21    1MR     8V -6.0000e+00    5uA  1.8000e-08  0.0000e+00  1.8000e-
08  1.3001e-08     4 ____AA_
      22 22    1MR     8V -6.0000e+00    5uA  1.5000e-08  0.0000e+00  1.5000e-
08  1.3001e-08     3 ____AA_
      22 23    1MR     8V -6.0000e+00    5uA  1.7000e-08  0.0000e+00  1.7000e-
08  1.3001e-08     3 ____AA_
      22 24    1MR     8V -6.0000e+00    5uA  1.8000e-08  1.0000e-09  1.7000e-
08  1.3001e-08     3 ____AA_
      22 25    1MR     8V -6.0000e+00    5uA  1.6000e-08  0.0000e+00  1.6000e-
08  1.3000e-08     3 ____AA_
      22 26    1MR     8V -6.0000e+00    5uA  1.8000e-08  0.0000e+00  1.8000e-
08  1.3001e-08     3 ____AA_
      22 27    1MR     8V -6.0000e+00    5uA  1.8000e-08  0.0000e+00  1.8000e-
08  1.3000e-08     4 ____AA_
      22 28    1MR     8V -6.0000e+00    5uA  1.8000e-08  1.0000e-09  1.7000e-
08  1.3000e-08     3 ____AA_
      22 29    1MR     8V -6.0000e+00    5uA  1.5000e-08  0.0000e+00  1.5000e-
08  1.3000e-08     3 ____AA_
```

```
      22 30   1MR    8V -6.0000e+00   5uA  1.6000e-08  0.0000e+00  1.6000e-
08  1.3000e-08    4 ____AA_
      22 31   1MR    8V -6.0000e+00   5uA  1.8000e-08  2.0000e-09  1.6000e-
08  1.3000e-08    2 ____AA_
      22 32   1MR    8V -6.0000e+00   5uA  1.6000e-08  0.0000e+00  1.6000e-
08  1.3000e-08    4 ____AA_
    CHECK COUNT =     1120    FAIL COUNT =       25
TEST   103733   RESULT   ==================================   13:50:24   ==>
FAIL***
DPU1        SLOT 12           BGR-024899     (AFC) IS DOUBTFUL
DPU1        SLOT 13           BGR-023709     (ADB) IS DOUBTFUL
DPU1        SLOT 16           BGR-023710     (BAB) IS DOUBTFUL
DPU1        SLOT 20           BGR-023711X02  (BFB) IS DOUBTFUL
DPU1        SLOT 5            BGR-024897     (ACA) IS DOUBTFUL
DPU1        SLOT 6            BGR-023715X02  (BDA) IS DOUBTFUL
DPU1        SLOT 7            BGR-024897     (ACA) IS DOUBTFUL
DPU1        SLOT 8            BGR-023715X02  (BDA) IS DOUBTFUL
DPU1        SLOT 9            BGR-024897     (ACA) IS DOUBTFUL
DPU1        SLOT 10           BGR-023715X02  (BDA) IS DOUBTFUL
TEST 140900 TH1 INIT TH ADJUSTMENT CHECK
INIT VIL OFFSET     PIN=  173 REG= 0X0930 LIMIT=   0.014 ,  -0.014 MEAS=  -
0.020 *** FAIL
    CHECK COUNT =    12288    FAIL COUNT =        1
TEST   140900   RESULT   ==================================   15:00:04   ==>
FAIL***
TEST 141100 TH1 DR OUTPUT VOLTAGE LINEARITY & RON/ROF CHECK
DATA_ID_NO.
0100000173.TPIN :  173 UPPER =  0.014 LOWER = -0.014 VIH DATA = -0.024 ***
FAIL
0500000173.TPIN :  173 UPPER = -1.954 LOWER = -2.046 VIL DATA = -1.839 ***
FAIL
0600000173.TPIN :  173 UPPER = -0.975 LOWER = -1.025 VIL DATA = -0.846 ***
FAIL
0700000173.TPIN :  173 UPPER =  0.014 LOWER = -0.014 VIL DATA =  0.105 ***
FAIL
THU         SLOT 13           BGR-024908     (ACA) IS BAD
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    CHECK COUNT =     5120    FAIL COUNT =        4
TEST   141100   RESULT   ====================================   15:00:26   ==>
FAIL***
TEST 141110 TH1 DR OUTPUT CURRENT & IMPEDANCE CHECK
DATA_ID_NO.
0000000173.TPIN :  173 UPPER = 55.653 LOWER = 44.347 Zo DATA = 76.590 ***
FAIL
0100000173.TPIN :  173 UPPER = 55.497 LOWER = 44.503 Zo DATA = 67.436 ***
FAIL
0200000173.TPIN :  173 UPPER = 52.765 LOWER = 47.235 Zo DATA = 95.421 ***
FAIL
0300000173.TPIN :  173 UPPER = 52.738 LOWER = 47.262 Zo DATA = 96.158 ***
FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
    CHECK COUNT =     2048    FAIL COUNT =        4
TEST   141110   RESULT   ====================================   15:00:43   ==>
FAIL***
TEST 141500 TH1 LIMITER FAIL MASK OPERATION CHECK
DATA_ID_NO.
3010000173 Pin: 173 H_EXPECT: PASS RESULT: FAIL *** FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
THU        SLOT 6            BGR-023948     (AJC) IS BAD
    CHECK COUNT =    35840    FAIL COUNT =        1
TEST   141500   RESULT   ====================================   15:02:38   ==>
FAIL***
TEST 144100 TH1 PRE I/O TIMING (NORMAL MODE) CHECK
DATA_ID_NO.
0101720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 76.181 I/O TIMING (Z-H) P_CHK
*** FAIL
1201720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 76.181 I/O TIMING (Z-L) F_CHK
*** FAIL
2101720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 73.819 I/O TIMING (H-Z) P_CHK
*** FAIL
2301720173.TPIN: 173 UPPER=126.181 LOWER= 73.819  I/O TIMING (H-Z)=NOT FIND
*** FAIL
3201720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 73.819 I/O TIMING (L-Z) F_CHK
```

*** FAIL
3301720173.TPIN: 173 UPPER=126.181 LOWER= 73.819 I/O TIMING (L-Z)=NOT FIND
*** FAIL
THU   SLOT 13   BGR-024908   (ACA) IS BAD
FPU1   SLOT 14   BMR-025625   (CBA) IS RELATED
    CHECK COUNT =   4100   FAIL COUNT =   6
TEST 144100 RESULT ================================== 15:05:01 ==>
FAIL***
TEST 144200 TH1 PRE DRE MINIMUM ON/OFF (NORMAL MODE) CHECK
DATA_ID_NO.
0101720173.TPIN: 173 T3=500.000 T4=565.000 T5=526.813 DRE ON (Z-H) P_CHK
*** FAIL
0301720173.TPIN: 173 T3=500.000 T4=565.000 T5=538.188 DRE ON (H-Z) P_CHK
*** FAIL
0501720173.TPIN: 173 UPPER=118.625 LOWER= 11.375 DRE ON TIME (Z-H)=NOT FOUND
*** FAIL
0601720173.TPIN: 173 UPPER=526.813 LOWER=473.187 T3 PHASE=504.219
*** FAIL
0701720173.TPIN: 173 UPPER=591.813 LOWER=538.188 T4 PHASE=NOT FOUND
*** FAIL
1201720173.TPIN: 173 T3=500.000 T4=565.000 T5=526.813 DRE ON (Z-L) F_CHK
*** FAIL
1401720173.TPIN: 173 T3=500.000 T4=565.000 T5=538.188 DRE ON (L-Z) F_CHK
*** FAIL
1501720173.TPIN: 173 UPPER=118.625 LOWER= 11.375 DRE ON TIME (Z-L)=NOT FOUND
*** FAIL
1601720173.TPIN: 173 UPPER=526.813 LOWER=473.187 T3 PHASE=504.375
*** FAIL
1701720173.TPIN: 173 UPPER=591.813 LOWER=538.188 T4 PHASE=NOT FOUND
*** FAIL
2101720173.TPIN: 173 T3=565.000 T4=500.000 T5=591.813 DRE OFF (Z-H) P_CHK
*** FAIL
2301720173.TPIN: 173 T3=565.000 T4=500.000 T5=473.187 DRE OFF (H-Z) P_CHK
*** FAIL
2501720173.TPIN: 173 UPPER=118.625 LOWER= 11.375 DRE OFF TIME (Z-H)=NOT FOUND
*** FAIL

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2601720173.TPIN:   173   UPPER=591.813   LOWER=538.188   T3   PHASE=596.250
*** FAIL
2701720173.TPIN:  173  UPPER=526.813  LOWER=473.187  T4  PHASE=NOT  FOUND
*** FAIL
3201720173.TPIN: 173 T3=565.000 T4=500.000 T5=591.813 DRE OFF (Z-L) F_CHK
*** FAIL
3501720173.TPIN: 173 UPPER=118.625 LOWER= 11.375 DRE OFF TIME (Z-L)=NOT FOUND
*** FAIL
3601720173.TPIN:   173   UPPER=591.813   LOWER=538.188   T3   PHASE=596.250
*** FAIL
3701720173.TPIN:  173  UPPER=526.813  LOWER=473.187  T4  PHASE=NOT  FOUND
*** FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
FPU1       SLOT 14           BMR-025625     (CBA) IS RELATED
    CHECK COUNT =     8204    FAIL COUNT =       19
TEST  144200  RESULT  ====================================  15:05:22  ==>
FAIL***
TEST 145100 TH1 I/O TIMING (NORMAL MODE) CHECK
DATA_ID_NO.
0101720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 52.681 I/O TIMING (Z-H) P_CHK
*** FAIL
0301720173.TPIN: 173 UPPER= 52.681 LOWER= 47.319  I/O TIMING (Z-H)=NOT FIND
*** FAIL
1201720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 52.681 I/O TIMING (Z-L) F_CHK
*** FAIL
1301720173.TPIN: 173 UPPER= 52.681 LOWER= 47.319  I/O TIMING (Z-L)=NOT FIND
*** FAIL
2101720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 97.319 I/O TIMING (H-Z) P_CHK
*** FAIL
2301720173.TPIN: 173 UPPER=102.681 LOWER= 97.319  I/O TIMING (H-Z)=NOT FIND
*** FAIL
3201720173.TPIN: 173 T3= 50.000 T4=100.000 T5= 97.319 I/O TIMING (L-Z) F_CHK
*** FAIL
3301720173.TPIN: 173 UPPER=102.681 LOWER= 97.319  I/O TIMING (L-Z)=NOT FIND
*** FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
```

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FPU1       SLOT 14           BMR-025625     (CBA) IS RELATED
    CHECK COUNT =     4100    FAIL COUNT =        8
TEST  145100  RESULT  ==================================  15:05:46  ==>
FAIL***
TEST 145120 TH1 I/O TIMING (VTT MODE) CHECK
DATA_ID_NO.
0100000173.TPIN: 173 T3= 50.000 T4=100.000 T5= 52.481 I/O TIMING (Z-H) P_CHK
*** FAIL
0300000173.TPIN: 173 UPPER= 52.481 LOWER= 47.519  I/O TIMING (Z-H)= 81.250
*** FAIL
1200000173.TPIN: 173 T3= 50.000 T4=100.000 T5= 52.481 I/O TIMING (Z-H) F_CHK
*** FAIL
1300000173.TPIN: 173 UPPER= 52.481 LOWER= 47.519  I/O TIMING (Z-L)=NOT FOUND
*** FAIL
2100000173.TPIN: 173 T3= 50.000 T4=100.000 T5= 97.519 I/O TIMING (H-Z) P_CHK
*** FAIL
2300000173.TPIN: 173 UPPER=102.481 LOWER= 97.519  I/O TIMING (H-Z)= 68.750
*** FAIL
3200000173.TPIN: 173 T3= 50.000 T4=100.000 T5= 97.519 I/O TIMING (L-Z) F_CHK
*** FAIL
3300000173.TPIN: 173 UPPER=102.481 LOWER= 97.519  I/O TIMING (L-Z)=NOT FOUND
*** FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
FPU1       SLOT 14           BMR-025625     (CBA) IS RELATED
    CHECK COUNT =     4100    FAIL COUNT =        8
TEST  145120  RESULT  ==================================  15:06:00  ==>
FAIL***
TEST 145200 TH1 DRE MINIMUM ON/OFF (NORMAL MODE) CHECK
DATA_ID_NO.
0101720173.TPIN: 173 T3= 50.000 T4= 56.500 T5= 52.681 DRE ON  (Z-H) P_CHK
*** FAIL
0301720173.TPIN: 173 T3= 50.000 T4= 56.500 T5= 53.819 DRE ON  (H-Z) P_CHK
*** FAIL
0501720173.TPIN: 173 UPPER= 11.863 LOWER=  1.137 DRE ON  TIME (Z-H)=NOT FOUND
*** FAIL
0601720173.TPIN:  173  UPPER=  52.681  LOWER=  47.319  T3  PHASE=NOT  FOUND
```

```
*** FAIL
0701720173.TPIN:  173  UPPER=  59.181  LOWER=  53.819  T4  PHASE=NOT  FOUND
*** FAIL
1201720173.TPIN: 173 T3= 50.000 T4= 56.500 T5= 52.681 DRE ON  (Z-L) F_CHK
*** FAIL
1401720173.TPIN: 173 T3= 50.000 T4= 56.500 T5= 53.819 DRE ON  (L-Z) F_CHK
*** FAIL
1501720173.TPIN: 173 UPPER= 11.863 LOWER=  1.137 DRE ON  TIME (Z-L)=NOT FOUND
*** FAIL
1601720173.TPIN:  173  UPPER=  52.681  LOWER=  47.319  T3  PHASE=NOT  FOUND
*** FAIL
1701720173.TPIN:  173  UPPER=  59.181  LOWER=  53.819  T4  PHASE=NOT  FOUND
*** FAIL
THU        SLOT 13           BGR-024908     (ACA) IS BAD
FPU1       SLOT 14           BMR-025625     (CBA) IS RELATED
    CHECK COUNT =     8198    FAIL COUNT =       10
TEST  145200  RESULT  ==================================  15:06:23  ==>
FAIL***
TEST 145220 TH1 DRE MINIMUM ON/OFF (VTT MODE) CHECK
DATA_ID_NO.
0100000173.TPIN: 173 T3= 50.000 T4= 55.000 T5= 51.411 DRE ON  (Z-H) P_CHK
*** FAIL
0300000173.TPIN: 173 T3= 50.000 T4= 55.000 T5= 53.589 DRE ON  (H-Z) P_CHK
*** FAIL
0500000173.TPIN: 173 UPPER=  7.822 LOWER=  2.177 DRE ON  TIME (Z-H)=NOT FOUND
*** FAIL
0600000173.TPIN:  173  UPPER=  51.411  LOWER=  48.589  T3  PHASE=NOT  FOUND
*** FAIL
0700000173.TPIN:  173  UPPER=  56.411  LOWER=  53.589  T4  PHASE=NOT  FOUND
*** FAIL
1200000173.TPIN: 173 T3= 50.000 T4= 55.000 T5= 51.411 DRE ON  (Z-L) F_CHK
*** FAIL
1400000173.TPIN: 173 T3= 50.000 T4= 55.000 T5= 53.589 DRE ON  (L-Z) F_CHK
*** FAIL
1500000173.TPIN: 173 UPPER=  7.822 LOWER=  2.177 DRE ON  TIME (Z-L)=NOT FOUND
*** FAIL
```

```
1600000173.TPIN:  173  UPPER=  51.411  LOWER=  48.589  T3  PHASE=NOT  FOUND
*** FAIL
1700000173.TPIN:  173  UPPER=  56.411  LOWER=  53.589  T4  PHASE=NOT  FOUND
*** FAIL
2100000173.TPIN: 173 T3= 55.000 T4= 50.000 T5= 56.411 DRE OFF (Z-H) P_CHK
*** FAIL
2300000173.TPIN: 173 T3= 55.000 T4= 50.000 T5= 48.589 DRE OFF (H-Z) P_CHK
*** FAIL
2500000173.TPIN: 173 UPPER=  7.822 LOWER=  2.177 DRE OFF TIME (Z-H)=NOT FOUND
*** FAIL
2600000173.TPIN:  173  UPPER=  56.411  LOWER=  53.589  T3  PHASE=NOT  FOUND
*** FAIL
2700000173.TPIN:  173  UPPER=  51.411  LOWER=  48.589  T4  PHASE=  18.750
*** FAIL
3200000173.TPIN: 173 T3= 55.000 T4= 50.000 T5= 56.411 DRE OFF (Z-L) F_CHK
*** FAIL
3400000173.TPIN: 173 T3= 55.000 T4= 50.000 T5= 48.589 DRE OFF (L-Z) F_CHK
*** FAIL
3500000173.TPIN: 173 UPPER=  7.822 LOWER=  2.177 DRE OFF TIME (Z-L)=NOT FOUND
*** FAIL
3600000173.TPIN:  173  UPPER=  56.411  LOWER=  53.589  T3  PHASE=NOT  FOUND
*** FAIL
3700000173.TPIN:  173  UPPER=  51.411  LOWER=  48.589  T4  PHASE=  18.750
*** FAIL
THU        SLOT 13          BGR-024908     (ACA) IS BAD
FPU1       SLOT 14          BMR-025625     (CBA) IS RELATED
    CHECK COUNT =     8204    FAIL COUNT =       20
TEST  145220  RESULT  ==================================  15:06:45  ==>
FAIL***
TEST 150100 FPU AFTER TH1 FUNCTION CHECK
     FPU anypin dutsyc Function Check
         fail count    pin            limit     error     stage
                1        Pin 173            100.00ps -276.72ns   800.00ns
FAIL***
    CHECK COUNT =     1538    FAIL COUNT =        1
TEST  150100  RESULT  ==================================  15:10:47  ==>
```

FAIL***

*　　DIAGNOSIS　　END　　AT　　2022/04/07　　16:05:57

*

SYSTEM　　RESULT　　**********>>

FAIL***