

## System Features

### AC Specification (Hardware)

	<b>DDR3</b>	<b>DDR2</b>	<b>DDR1</b>	<b>SDRAM</b>	<b>pSRAM</b>	<b>NandFlash</b>	<b>NorFlash</b>	<b>SPI NorFlash</b>	<b>eMMC</b>
<b>Test Frequency</b>	Up to 667M hz	Up to 400Mhz	Up to 200Mhz	Up to 166Mhz	~	Up to 200MHz (Async) 166 MHz (Sync) 200 MHz (Toggle)	Up to 200MHz	fC up to 100MHz fR, fC2, fT2 up to 50MHz fT up to 70MHz	Up to 50MHz
<b>Switching Data Rate</b>	800Mbps to 1600 Mbps	400Mbps to 800Mbps	266Mbps to 400Mbps	200Mbps to 333Mbps	~	20MB/s to 166MB/s 200MB/s (Toggle)	Async: 70ns (min)	Up to 200Mbps	Up to 100MB/s
<b>I/O Interface</b>	SSTL_15, Class I & Class II	SSTL_18, Class I & Class II	SSTL_25, Class I & Class II ( For mobile DDR1, 1.8V LVCMOS )	3V LVTTL ( For mobile SDRAM, 1.8V LVCMOS )	3V LVTTL	ONFI 1.0, ONFI 2.0, ONFI 3.0, Toggle Nand Flash	CFI	SPI	MMC V4.41
<b>Address Depth</b>	16/16/3 per site, up to 16 sites				26bit, up to 16 sites	Device size: 65536 blocks Block size: 8192 pages Page size: 32768 columns	63 32 - Kword Main Blocks, 8 4 - Kword Boot Blocks, Top Boot/Bottom Boot	16-bit 64K-byte block 8-bit sector/block 14-bit address/sector	Device density up to 2TB Block length up to 2048 byte. 14-bit erase groups addressing 8-bit write protect group addressing

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<b>Data Depth</b>	Supports 8/16/32 bit IC devices				Supports 16 bit IC devices	x8, x16 per DUT site	x8 and x16 per DUT site	x8 per DUT site	x1, x4, x8 per DUT site
<b>Control Signal</b>	4 CS/ RAS/ CAS/ WE/ 2 CKE/ 2 ODT/ RST/ 2ZQ	4 CS/ RAS/ CAS/ WE/ 2 CKE/ 2 ODT	4 CS/ RAS/ CAS/ WE/ 2 CKE	CE1/ CE2/ UB/ LB/ WE	Control Lines (Async): 4 CS#, 4 RYBY; 1 RE#, 1 ALE, 1 WP#, 1 CLE, 1 WE# in dual channel Control Lines (Sync): 4 CS#, 4 RYBY; 1 W/R#, 1 ALE, 1 WP#, 1 CLE, 1 CLK, 1 DQS in dual channel Control Lines (Toggle): 4CS#, 4RYBY, 1CLE, 1ALE, 1RE, 1WR, 1WP#, 1DQS in dual channel	Control Lines: 4 CE-, OE-, WE-, WP-, RST-		1 CS#, 1 SCLK, 1 SI, 1 WP	1 CLK 1 CMD

	<b>DDR3</b>	<b>DDR2</b>	<b>DDR1</b>	<b>SDRAM</b>	<b>pSRAM</b>	<b>NandFlash</b>	<b>NorFlash</b>	<b>SPI NorFlash</b>	<b>eMMC</b>
<b>Programmable Timing</b>	tRCD, tRP, tBL, tCL , tAL, tWR , tWL, tRL, tRRP, tFAW , tWTR , tRAS , tRRD , tRTP , tMRD , tRFC, tRC, tMOD, tCWL	tRCD, tRP, tBL, tCL , tAL, tAL, tWR , tWL, tRL, tRRP, tFAW , tWTR , tWTR , tRAS , tRAS , tRAS , tRTP , tRRD , tRTP , tMRD , tRFC, tRFC, tRC	tRCD, tRP, tBL, tCL , tAL, tAL, tAL, tWR , tWR , tRL, tRRP, tFAW , tWTR , tWTR , tRAS , tRAS , tRAS , tRTP , tRRD , tRTP , tMRD , tRFC, tRFC, tRC	tRCD, tRP, tBL, tCL , tAL, tAL, tAL, tWR , tWR , tRL, tRRP, tFAW , tWTR , tWTR , tRAS , tRAS , tRAS , tRTP , tRRD , tRTP , tMRD , tRFC, tRFC, tRC	tRC, tAA, tCO, tOE, tBA, tWC, tCW, tWR, tAS, tAW, tBW, tWP, tDW, tDH, tOW	Async Programmable Timing: tCLS, tCLH, tALS, tALH, tWP, tWH, tDS, tDH, tDS, tDH, tWC, tADL, tCH, tWW, tCS, tRP, tRC, tREA, tRR, tOH, tWHR, tAR, tWB, tREH, tRHW, tBERS, tR, tPROG  Sync Programmable Timing: tADL, tCAD, tCALS, tDS, tCCS, tDQSS, tWB, tWW, tDQSCK, tRHW, tWHR, tWPRE, tWPST, tBERS, tPROG, tR  Toggle Programmable Timing: tADL, tCALS, tCS, tCH, tAR, tRR, tWB, tWHR, tWC, tWP, tWW, tWHR2, tWPRE, tCDQSS, tCDQSH, tWPST, tWPSTH, tRPRE, tDQSRE, tRPST, tRPSTH, tBERS, tR, tPROG, tDS	tAVAV, tGLQV, tGHQZ, tAVQV, tWHQV1, tWHQV2, tWHQV3, tWHRH1, tWHRH2, tWP, tELWL, tDVWH, tAVWH, tWHEH, tWHDX, tWHAX, tWHWL	tSHSL_Rd, tSHSL_Wr, tWHSLSL, tSHWL, tDVCH_s(fc), tDVCH_S(fr), tDVCH_S(ft), tBP, tPP, tWPS, tWSR, tW, tSE, tBE32, tBE64, tCE	tISU, NCC, NCD, NCP, NRC, NSC, NWR Boot operation: tBD,tBA Identification: NID

## DC Specification (Hardware)

	<b>DDR3/ DDR2/ DDR1</b>	<b>SDRAM</b>	<b>pSRAM</b>	<b>NandFlash/ NorFlash/SPI NorFlash/ eMMC</b>
<b>Variable Power Supplies</b>	Vdd: 1.2V to 4.0V, resolution 0.01V, 15A, +/- 2% Vtt: $\frac{1}{2}$ of Vdd, 3A Vref: 0.6V to 2.0V, resolution 0.01V, 30mA, +/- 2%	Vdd: 1.2V to 4.0V, resolution 0.01V, 15A, +/- 2% Vref: 0.6V to 2.0V, resolution 0.01V, 30mA, +/- 2%	Vdd: 1.2V to 4.0V, resolution 0.01V, 15A, +/- 2%	Vdd: 1.20V to 3.8V, resolution 0.01V, 4A, +/- 2%, per DUT site
<b>Icc Measurement (Based on measurement of each site)</b>	<p>Operating Icc Measurement:            R1: 0 - 3A (+/- 50mA)            R2: 3 - 10A (+/- 100 mA)</p> <p>Stand-by Icc Measurement:            R1: 0uA - 10uA, +/- 1uA            R2: 10uA - 100uA, +/- 2uA            R3: 100uA - 1mA, +/- 25uA            R4: 1mA - 40mA, +/- 450uA</p>			
<b>Leakage Current Measurement</b>	<p>R1: 0uA – 10uA, +/- 1uA            R2: 10uA – 100uA, +/- 2uA            R3: 100uA – 1mA, +/- 25uA            R4: 1mA – 40mA, +/- 450uA</p> <p>(Based on measurement of each site)</p>			
<b>DC Tests</b>	DC Open, Shorts/Leakage, Icc			DC Shorts/Leakage, Icc

## System and Software Features

	<b>DDR3/ DDR2/ DDR1</b>	<b>SDRAM</b>	<b>pSRA M</b>	<b>NandFlash</b>	<b>NorFlash</b>	<b>SPI NorFlash</b>	<b>eMMC</b>
<b>System and Software Features</b>	AC/ Icc tests		AC/ DC parametric tests				
	~		Built in Icc patterns include sequential read operating current, program operating current, erase operating current and stand-by current (TTL)	Built in Icc patterns include read operating current, program operating current, erase operating current and stand-by current	Built in Icc patterns include block erase, fast read, page program and stand-by current	Built in Icc patterns include block erase, fast read, page program	
			Support leakage test		TBD		
	~		Supports both large block and small block architecture  Supports Block/ Page/ Column modes  Supports cache read, sequential read and copy back  Flexible bad block management available for read bad block	Supports both top boot and bottom boot architecture  Supports Block/Column modes	Supports serial 1x, 2x, 4x and parallel I/O mode  Supports both SDR and DDR	Support 1x, 2x, 4x data width  Supports both SDR and DDR	
	~		Supports 12V fast production programming		~		

	<b>DDR3/ DDR2/ DDR1</b>	<b>SDRAM</b>	<b>pSRAM</b>	<b>NandFlash</b>	<b>NorFlash</b>	<b>SPI NorFlash</b>	<b>eMMC</b>
<b>System and Software Features</b>	Over 35 industry standard AC test patterns available		Over 35 industry standard AC test patterns available	Over 20 AC timing parameters for AC parametric testing (Async)	Over 15 industry standard AC test patterns available	Over 10 industry standard AC test patterns available	TBD
			Over 15 AC timing parameters for AC parametric testing (Sync)	Over 15 AC timing parameters for AC parametric testing		Over 15 AC timing parameters for AC parametric testing	
			Support both text and graphical result display				Support both text and graphical result display
	Support Auto Calibration Feature	~					
			Support Single IC and MCP device form factors				Support Single IC and MCP device form factors
			For TCII-1200 MCP, support 16 DUT Sites in x8, 8 DUT Sites in x16, 4 DUT Sites in x32 parallel tests For TCIII-1200 MCP, support 64 DUT Sites in x8, 32 DUT Sites in x16, 16 DUT Sites in x32 parallel tests				For TCII-1200 MCP, support 16 DUT Sites in x8, 8 DUT Sites in x16, 4 DUT Sites in x32 parallel tests For TCIII-1200 MCP, support 64 DUT Sites in x8, 32 DUT Sites in x16, 16 DUT Sites in x32 parallel tests
	S.A.T. optional	~					
			Hot Chamber and Handler Interface optional				Hot Chamber and Handler

		Interface optional
<b>Min. Control PC</b>	Windows XP+ and networking interface	Windows XP+ and networking interface
<b>Test Unit Dimensions</b>	For TCII-1200 MCP: 450mm x 295mm x 245mm (W x D x H) For TCIII-1200 MCP: 1000mm x 600mm x 360mm (W x D x H)	For TCII-1200 MCP: 450mm x 295mm x 245mm (W x D x H) For TCIII-1200 MCP: 1000mm x 600mm x 360mm (W x D x H)
<b>AC Power Supply</b>	110 – 240 VAC, 50/60 Hz	110 – 240 VAC, 50/60 Hz