

Successfully removed tdl files

Successfully started file /tmp/advantest/\_default/hardware.tdl

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\* DIAGNOSIS VERSION R2.03 (for viewpoint R8.16 or later) \*

\* SYSTEM NAME T6373

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\* DIAGNOSIS STARTED AT 2022/11/22 20:09:39 \*

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----- SYSTEM CONFIGURATION INFORMATION -----

PIN CONFIGURATION

MAINFRAME : 1 - 256  
TH1 [CTD ]: 1 - 256  
LCD : 1 - 2304  
RVS : 1 - 64

DPU CONFIGURATION

UDC CH : 1 - 4  
MDC CH : 1 - 24  
PPS CH : 1 - 16  
HVDC CH : 1 - 144  
LINE FREQUENCY : 60Hz  
DMM MODEL : R6581T

SQPG CONFIGURATION

MAX VGC : 4MW  
MAX CTB : 32MW  
MAX TTB : 32MW

LCD CONFIGURATION

AQM BLOCK : 1 - 26  
GREF CH : 1 - 6  
IDDQ CH : 1 - 16

HSIF CONFIGURATION

HSIF CH : 1 - 8  
HI-FIX TYPE : 256AI

----- DIAGNOSIS INFORMATION -----

DIAGNOSIS MODE : NORMAL

DIAGNOSIS TEST NUMBER : 192150 - 192150

DIAGNOSIS SPEC. : 100.0

DIAGNOSIS REPEAT COUNT : 1

DIAGNOSIS PIN INFORMATION

MAINFRAME : 1 - 256

TH1 : 1 - 256

LCD : 1 - 2304

RVS : 1 - 64

DIAGNOSIS DPU INFORMATION

UDC CH : 1 - 4

MDC CH : 1 - 24

PPS CH : 1 - 16

HVDC CH : 1 - 144

DIAGNOSIS LCD INFORMATION

AQM BLOCK : 1 - 26

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TEST 192150 HSIF PIN PB CONNECTION CHECK

DPU initialization data successfully recovered.

TEST 192150 RESULT ----- 20:09:41 --> \*\*\*PASS

\* DIAGNOSIS END AT 2022/11/22 20:10:23

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SYSTEM RESULT .....>> \*\*\*PASS

Successfully removed tdl files

Successfully started file /tmp/advantest/\_default/hardware.tdl

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\* DIAGNOSIS VERSION R2.03 (for viewpoint R8.16 or later) \*

\* SYSTEM NAME T6373

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\* DIAGNOSIS STARTED AT 2022/11/22 20:10:47 \*

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----- SYSTEM CONFIGURATION INFORMATION -----

PIN CONFIGURATION

MAINFRAME : 1 - 256

TH1 [CTD ]: 1 - 256

LCD : 1 - 2304

RVS : 1 - 64

DPU CONFIGURATION

UDC CH : 1 - 4  
MDC CH : 1 - 24  
PPS CH : 1 - 16  
HVDC CH : 1 - 144  
LINE FREQUENCY : 60Hz  
DMM MODEL : R6581T

SQPG CONFIGURATION

MAX VGC : 4MW  
MAX CTB : 32MW  
MAX TTB : 32MW

LCD CONFIGURATION

AQM BLOCK : 1 - 26  
GREF CH : 1 - 6  
IDDQ CH : 1 - 16

HSIF CONFIGURATION

HSIF CH : 1 - 8  
HI-FIX TYPE : 256AI

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----- DIAGNOSIS INFORMATION -----

DIAGNOSIS MODE : NORMAL  
DIAGNOSIS TEST NUMBER : -1 - -1  
DIAGNOSIS SPEC. : 100.0  
DIAGNOSIS REPEAT COUNT : 1

DIAGNOSIS PIN INFORMATION

MAINFRAME : 1 - 256  
TH1 : 1 - 256  
LCD : 1 - 2304  
RVS : 1 - 64

DIAGNOSIS DPU INFORMATION

UDC CH : 1 - 4  
MDC CH : 1 - 24  
PPS CH : 1 - 16  
HVDC CH : 1 - 144

DIAGNOSIS LCD INFORMATION

AQM BLOCK : 1 - 26  
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TEST 140000 TH1 PB FLAG READ CHECK  
TEST 140000 RESULT ----- 20:10:47 --> \*\*\*PASS  
TEST 141000 TH1 PIN/CW/PCON PB CONNECTION CHECK  
DPU initialization data successfully recovered.  
TEST 141000 RESULT ----- 20:11:28 --> \*\*\*PASS  
TEST 184000 LCD PIN PB CONNECTION CHECK  
HVDPU initialization data successfully recovered.  
TEST 184000 RESULT ----- 20:14:07 --> \*\*\*PASS  
TEST 192150 HSIF PIN PB CONNECTION CHECK  
TEST 192150 RESULT ----- 20:14:08 --> \*\*\*PASS  
TEST 101003 DPU IFL REG. W/R CHECK  
TEST 101003 RESULT ----- 20:14:08 --> \*\*\*PASS  
TEST 101058 DPU IFL BUSY CHECK  
TEST 101058 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101103 DPU IFA REG. W/R CHECK  
TEST 101103 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101203 DPU UDC\_C REG. W/R CHECK  
TEST 101203 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101403 DPU MDC\_C REG. W/R CHECK  
TEST 101403 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101458 DPU MDC\_C BUSY CHECK  
TEST 101458 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101503 DPU MDC REG. W/R CHECK  
TEST 101503 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101563 DPU MDC MEAS DSP/ALU CHECK  
TEST 101563 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 101803 DPU PPS\_C REG. W/R CHECK  
TEST 101803 RESULT ----- 20:14:09 --> \*\*\*PASS  
TEST 103328 DPU UDC VSIM VS ACCURACY CHECK  
TEST 103328 RESULT ----- 20:14:12 --> \*\*\*PASS  
TEST 103333 DPU UDC VSIM IM ACCURACY CHECK  
TEST 103333 RESULT ----- 20:14:17 --> \*\*\*PASS  
TEST 103338 DPU UDC VSIM CLAMP ACCURACY CHECK  
TEST 103338 RESULT ----- 20:14:25 --> \*\*\*PASS  
TEST 103343 DPU UDC ISVM IS ACCURACY CHECK  
TEST 103343 RESULT ----- 20:14:43 --> \*\*\*PASS

TEST 103348 DPU           UDC    ISVM VM            ACCURACY CHECK  
 TEST 103348 RESULT ----- 20:14:48 --> \*\*\*PASS  
 TEST 103353 DPU           UDC    ISVM CLAMP        ACCURACY CHECK  
 TEST 103353 RESULT ----- 20:14:53 --> \*\*\*PASS  
 TEST 103358 DPU           UDC    MVM  VM            ACCURACY CHECK  
 TEST 103358 RESULT ----- 20:14:57 --> \*\*\*PASS  
 TEST 103528 DPU           MDC    VSIM VS           ACCURACY CHECK  
 TEST 103528 RESULT ----- 20:15:03 --> \*\*\*PASS  
 TEST 103533 DPU           MDC    VSIM IM           ACCURACY CHECK  
 TEST 103533 RESULT ----- 20:15:34 --> \*\*\*PASS  
 TEST 103538 DPU           MDC    VSIM CLAMP        ACCURACY CHECK  
 TEST 103538 RESULT ----- 20:15:52 --> \*\*\*PASS  
 TEST 103543 DPU           MDC    ISVM IS            ACCURACY CHECK  
 TEST 103543 RESULT ----- 20:16:59 --> \*\*\*PASS  
 TEST 103548 DPU           MDC    ISVM VM            ACCURACY CHECK  
 TEST 103548 RESULT ----- 20:17:07 --> \*\*\*PASS  
 TEST 103553 DPU           MDC    ISVM CLAMP        ACCURACY CHECK  
 TEST 103553 RESULT ----- 20:17:17 --> \*\*\*PASS  
 TEST 103828 DPU           PPS    VSIM VS            ACCURACY CHECK  
 TEST 103828 RESULT ----- 20:17:27 --> \*\*\*PASS  
 TEST 103833 DPU           PPS    VSIM IM            ACCURACY CHECK  
 TEST 103833 RESULT ----- 20:20:30 --> \*\*\*PASS  
 TEST 103838 DPU           PPS    VSIM CLAMP        ACCURACY CHECK  
 TEST 103838 RESULT ----- 20:21:42 --> \*\*\*PASS  
 TEST 103863 DPU           PPS    VSVM VS            ACCURACY CHECK  
 TEST 103863 RESULT ----- 20:21:52 --> \*\*\*PASS  
 TEST 103868 DPU           PPS    VSVM VM            ACCURACY CHECK  
 TEST 103868 RESULT ----- 20:22:12 --> \*\*\*PASS  
 TEST 104028 DPU           DPU-PG(SELF)            CHECK  
 TEST 104028 RESULT ----- 20:22:12 --> \*\*\*PASS  
 TEST 104303 DPU           UDC    VSIM IM            SETTLING CHECK  
 TEST 104303 RESULT ----- 20:22:35 --> \*\*\*PASS  
 TEST 104313 DPU           UDC    GUARD            ALARM    CHECK  
 TEST 104313 RESULT ----- 20:22:38 --> \*\*\*PASS  
 TEST 104343 DPU           UDC    PRECHECK  
 TEST 104343 RESULT ----- 20:22:38 --> \*\*\*PASS

|                    |              |          |                |
|--------------------|--------------|----------|----------------|
| TEST 104503 DPU    | MDC          | VSIM IM  | SETTLING CHECK |
| TEST 104503 RESULT | -----        | 20:23:02 | --> ***PASS    |
| TEST 104513 DPU    | MDC          | GUARD    | ALARM CHECK    |
| TEST 104513 RESULT | -----        | 20:23:05 | --> ***PASS    |
| TEST 104533 DPU    | MDC          | DUT      | MASK CHECK     |
| TEST 104533 RESULT | -----        | 20:23:05 | --> ***PASS    |
| TEST 104543 DPU    | MDC          | PRECHECK |                |
| TEST 104543 RESULT | -----        | 20:23:09 | --> ***PASS    |
| TEST 104803 DPU    | PPS          | VSIM IM  | SETTLING CHECK |
| TEST 104803 RESULT | -----        | 20:23:13 | --> ***PASS    |
| TEST 104813 DPU    | PPS          | GUARD    | ALARM CHECK    |
| TEST 104813 RESULT | -----        | 20:23:19 | --> ***PASS    |
| TEST 104823 DPU    | PPS          | SPIKE    | CHECK          |
| TEST 104823 RESULT | -----        | 20:23:36 | --> ***PASS    |
| TEST 104843 DPU    | PPS          | PRECHECK |                |
| TEST 104843 RESULT | -----        | 20:23:53 | --> ***PASS    |
| TEST 105003 HVDPDU | IFL          | REG. W/R | CHECK          |
| TEST 105003 RESULT | -----        | 20:23:53 | --> ***PASS    |
| TEST 105008 HVDPDU | IFL          | BUSY     | CHECK          |
| TEST 105008 RESULT | -----        | 20:23:54 | --> ***PASS    |
| TEST 105013 HVDPDU | IFA          | REG. W/R | CHECK          |
| TEST 105013 RESULT | -----        | 20:23:54 | --> ***PASS    |
| TEST 105038 HVDPDU | DPU-PG(SELF) |          | CHECK          |
| TEST 105038 RESULT | -----        | 20:23:54 | --> ***PASS    |
| TEST 105045 HVDPDU | MDC_C        | REG. W/R | CHECK          |
| TEST 105045 RESULT | -----        | 20:23:54 | --> ***PASS    |
| TEST 105050 HVDPDU | MDC_C        | BUSY     | CHECK          |
| TEST 105050 RESULT | -----        | 20:23:54 | --> ***PASS    |
| TEST 105120 HVDPDU | HVDC         | REG. W/R | CHECK          |
| TEST 105120 RESULT | -----        | 20:23:56 | --> ***PASS    |
| TEST 105420 HVDPDU | HVDC         | MVM      | ACCURACY CHECK |
| TEST 105420 RESULT | -----        | 20:23:56 | --> ***PASS    |
| TEST 105430 HVDPDU | HVDC         | VSIM VS  | ACCURACY CHECK |
| TEST 105430 RESULT | -----        | 20:23:57 | --> ***PASS    |
| TEST 105440 HVDPDU | HVDC         | ISVM IS  | ACCURACY CHECK |
| TEST 105440 RESULT | -----        | 20:24:04 | --> ***PASS    |

TEST 105450 HVDPU HVDC VSIM IM ACCURACY CHECK  
TEST 105450 RESULT ----- 20:24:10 --> \*\*\*PASS  
TEST 105460 HVDPU HVDC VSIM CLAMP ACCURACY CHECK  
TEST 105460 RESULT ----- 20:24:15 --> \*\*\*PASS  
TEST 105470 HVDPU HVDC ISVM CLAMP ACCURACY CHECK  
TEST 105470 RESULT ----- 20:24:15 --> \*\*\*PASS  
TEST 105610 HVDPU HVDC VSIM IM SETTLING CHECK  
TEST 105610 RESULT ----- 20:24:16 --> \*\*\*PASS  
TEST 105650 HVDPU HVDC PRECHECK  
TEST 105650 RESULT ----- 20:24:25 --> \*\*\*PASS  
TEST 105660 HVDPU HVDC HGND INTERNAL CONNECT CHECK  
TEST 105660 RESULT ----- 20:24:25 --> \*\*\*PASS  
TEST 105670 HVDPU HVDC OUT RELAY GND CONNECT CHECK  
SQPG initialization data successfully recovered.  
TEST 105670 RESULT ----- 20:24:28 --> \*\*\*PASS  
TEST 110100 SNC REGISTER READ/WRITE CHECK  
TEST 110100 RESULT ----- 20:24:28 --> \*\*\*PASS  
TEST 110200 SNC REFCLK CHECK  
TEST 110200 RESULT ----- 20:24:35 --> \*\*\*PASS  
TEST 110300 SNC REFCLK PAUSE CHECK  
TEST 110300 RESULT ----- 20:24:39 --> \*\*\*PASS  
TEST 110400 SNC LOOP TPD MEASUREMENT CHECK  
TEST 110400 RESULT ----- 20:24:39 --> \*\*\*PASS  
TEST 120000 SQPG PGIF REGISTER READ/WRITE CHECK  
TEST 120000 RESULT ----- 20:24:39 --> \*\*\*PASS  
TEST 120010 SQPG SQPG REGISTER READ/WRITE CHECK  
TEST 120010 RESULT ----- 20:24:39 --> \*\*\*PASS  
TEST 120020 SQPG TTB/DFM PIN MAP CHECK  
TEST 120020 RESULT ----- 20:24:40 --> \*\*\*PASS  
TEST 120025 SQPG LCD TTB/DC/DFM PIN MAP CHECK  
TEST 120025 RESULT ----- 20:24:40 --> \*\*\*PASS  
TEST 120027 SQPG LCD TTB/DC/DFM PIN GROUP CHECK  
TEST 120027 RESULT ----- 20:25:42 --> \*\*\*PASS  
TEST 120030 SQPG EVENT TTB PIN MAP CHECK  
TEST 120030 RESULT ----- 20:25:42 --> \*\*\*PASS  
TEST 120040 SQPG TTB/DFM REGISTER READ/WRITE CHECK BY PHYSICAL PIN

TEST 120040 RESULT ----- 20:25:43 --> \*\*\*PASS  
TEST 120045 SQPG LCD TTB/DC/DFM REGISTER READ/WRITE CHECK BY  
PHYSICAL PIN  
TEST 120045 RESULT ----- 20:25:46 --> \*\*\*PASS  
TEST 120050 SQPG TTB/DFM REGISTER READ/WRITE CHECK BY LOGICAL PIN  
TEST 120050 RESULT ----- 20:26:05 --> \*\*\*PASS  
TEST 120055 SQPG LCD TTB/DC/DFM REGISTER READ/WRITE CHECK BY  
LOGICAL PIN  
TEST 120055 RESULT ----- 20:27:03 --> \*\*\*PASS  
TEST 120057 SQPG LCD TTB/DC/DFM REGISTER READ/WRITE CHECK BY GROUP  
PIN  
TEST 120057 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120060 SQPG EVENT TTB REGISTER READ/WRITE CHECK BY PHYSICAL PIN  
TEST 120060 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120070 SQPG EVENT TTB REGISTER READ/WRITE CHECK BY LOGICAL PIN  
TEST 120070 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120080 SQPG STE/DFM MEMORY SENSE CHECK  
TEST 120080 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120100 SQPG RATE MEMORY READ/WRITE CHECK  
TEST 120100 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120110 SQPG VGC MEMORY READ/WRITE CHECK  
TEST 120110 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120120 SQPG CTB MEMORY READ/WRITE CHECK  
TEST 120120 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120130 SQPG TTB MEMORY READ/WRITE CHECK  
TEST 120130 RESULT ----- 20:27:05 --> \*\*\*PASS  
TEST 120135 SQPG LCD TTB MEMORY READ/WRITE CHECK  
TEST 120135 RESULT ----- 20:27:06 --> \*\*\*PASS  
TEST 120137 SQPG LCD TTB MEMORY READ/WRITE CHECK 2  
TEST 120137 RESULT ----- 20:27:08 --> \*\*\*PASS  
TEST 120140 SQPG EVENT TTB MEMORY READ/WRITE CHECK  
TEST 120140 RESULT ----- 20:27:08 --> \*\*\*PASS  
TEST 120150 SQPG UBM MEMORY READ/WRITE CHECK  
TEST 120150 RESULT ----- 20:27:21 --> \*\*\*PASS  
TEST 120200 SQPG STE TRANSFER CHECK BY PHYSICAL PIN  
TEST 120200 RESULT ----- 20:27:38 --> \*\*\*PASS

TEST 120205 SQPG LCD TTB TRANSFER CHECK BY PHYSICAL PIN(SHORT)  
TEST 120205 RESULT ----- 20:27:40 --> \*\*\*PASS  
TEST 120210 SQPG STE TRANSFER CHECK BY LOGICAL PIN  
TEST 120210 RESULT ----- 20:27:46 --> \*\*\*PASS  
TEST 120215 SQPG LCD TTB TRANSFER CHECK BY LOGICAL PIN(SHORT)  
TEST 120215 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120220 SQPG EVENT TTB TRANSFER CHECK BY PHYSICAL PIN  
TEST 120220 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120230 SQPG EVENT TTB TRANSFER CHECK BY LOGICAL PIN  
TEST 120230 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120250 SQPG ERROR INSTRUCTION TRANS CHECK  
TEST 120250 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120500 SQPG START CHECK  
TEST 120500 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120510 SQPG STOP CHECK  
TEST 120510 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120520 SQPG INTERRUPT CHECK  
TEST 120520 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120600 SQPG CTRL OUTPUT CHECK  
TEST 120600 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120610 SQPG CTB PATTERN OUTPUT CHECK  
TEST 120610 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120620 SQPG TTB PATTERN OUTPUT CHECK  
TEST 120620 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120625 SQPG LCD TTB PATTERN OUTPUT CHECK  
TEST 120625 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120650 SQPG TTB PATMUX PATTERN OUTPUT CHECK 1  
TEST 120650 RESULT ----- 20:27:47 --> \*\*\*PASS  
TEST 120660 SQPG TTB PATMUX PATTERN OUTPUT CHECK 2  
TEST 120660 RESULT ----- 20:27:50 --> \*\*\*PASS  
TEST 120700 SQPG CPE WINDOW SYNC CHECK  
TEST 120700 RESULT ----- 20:27:50 --> \*\*\*PASS  
TEST 121000 SQPG RATE PERIOD CHECK  
TEST 121000 RESULT ----- 20:27:51 --> \*\*\*PASS  
TEST 121100 SQPG REPEAT CHECK  
TEST 121100 RESULT ----- 20:27:52 --> \*\*\*PASS

TEST 121110 SQPG CONTINUE MODE CHECK  
TEST 121110 RESULT ----- 20:27:52 --> \*\*\*PASS  
TEST 121150 SQPG SPA COMBINATION CHECK  
TEST 121150 RESULT ----- 20:27:53 --> \*\*\*PASS  
TEST 121200 SQPG PAUSE CHECK  
TEST 121200 RESULT ----- 20:27:53 --> \*\*\*PASS  
TEST 121210 SQPG PAUSE TIMER CHECK  
TEST 121210 RESULT ----- 20:27:53 --> \*\*\*PASS  
TEST 121300 SQPG OUT FIFO READ/WRITE CHECK  
TEST 121300 RESULT ----- 20:27:55 --> \*\*\*PASS  
TEST 121310 SQPG OUT HOLD CHECK  
TEST 121310 RESULT ----- 20:27:56 --> \*\*\*PASS  
TEST 121320 SQPG OUT ERROR MASK CHECK  
TEST 121320 RESULT ----- 20:27:56 --> \*\*\*PASS  
TEST 121330 SQPG OUT TIME OUT CHECK  
TEST 121330 RESULT ----- 20:27:58 --> \*\*\*PASS  
TEST 121500 SQPG JNI LOOP CHECK  
TEST 121500 RESULT ----- 20:27:58 --> \*\*\*PASS  
TEST 121510 SQPG JEC LOOP CHECK  
TEST 121510 RESULT ----- 20:27:59 --> \*\*\*PASS  
TEST 121800 SQPG VGC INDEX STACK ERROR CHECK  
TEST 121800 RESULT ----- 20:27:59 --> \*\*\*PASS  
TEST 121810 SQPG VGC CACHE ERROR CHECK  
TEST 121810 RESULT ----- 20:27:59 --> \*\*\*PASS  
TEST 121820 SQPG VGC REGISTER LOOP ERROR CHECK  
TEST 121820 RESULT ----- 20:27:59 --> \*\*\*PASS  
TEST 122000 SQPG TTB START ADDRESS LOAD CHECK  
TEST 122000 RESULT ----- 20:27:59 --> \*\*\*PASS  
TEST 122010 SQPG TTB START ADDRESS CHECK  
TEST 122010 RESULT ----- 20:28:00 --> \*\*\*PASS  
TEST 122100 SQPG PC BANK CONTROL CHECK 0  
TEST 122100 RESULT ----- 20:28:00 --> \*\*\*PASS  
TEST 122110 SQPG PC BANK CONTROL CHECK 1  
TEST 122110 RESULT ----- 20:28:00 --> \*\*\*PASS  
TEST 122120 SQPG PC BANK CONTROL CHECK 2  
TEST 122120 RESULT ----- 20:28:01 --> \*\*\*PASS

TEST 122130 SQPG PC BANK CONTROL CHECK 3  
TEST 122130 RESULT ----- 20:28:01 --> \*\*\*PASS  
TEST 122140 SQPG PC BANK CONTROL CHECK 4  
TEST 122140 RESULT ----- 20:28:01 --> \*\*\*PASS  
TEST 122150 SQPG PC BANK CONTROL CHECK 5  
TEST 122150 RESULT ----- 20:28:01 --> \*\*\*PASS  
TEST 122200 SQPG CTB READ BANK CHECK  
TEST 122200 RESULT ----- 20:28:01 --> \*\*\*PASS  
TEST 122210 SQPG TTB READ BANK CHECK  
TEST 122210 RESULT ----- 20:28:02 --> \*\*\*PASS  
TEST 122230 SQPG TTB PATMUX READ BANK CHECK  
TEST 122230 RESULT ----- 20:28:02 --> \*\*\*PASS  
TEST 122300 SQPG CTB READ PC CHECK  
TEST 122300 RESULT ----- 20:28:03 --> \*\*\*PASS  
TEST 122310 SQPG TTB READ PC CHECK  
TEST 122310 RESULT ----- 20:28:04 --> \*\*\*PASS  
TEST 122315 SQPG LCD TTB READ PC CHECK  
TEST 122315 RESULT ----- 20:28:06 --> \*\*\*PASS  
TEST 122330 SQPG TTB PATMUX READ PC CHECK  
TEST 122330 RESULT ----- 20:28:07 --> \*\*\*PASS  
TEST 122350 SQPG TTB RBANK CHECK2  
TEST 122350 RESULT ----- 20:28:07 --> \*\*\*PASS  
TEST 122800 SQPG CTB PARITY GENERATOR & PARITY ERROR CHECK  
TEST 122800 RESULT ----- 20:28:07 --> \*\*\*PASS  
TEST 122810 SQPG TTB PARITY GENERATOR & PARITY ERROR CHECK  
TEST 122810 RESULT ----- 20:28:12 --> \*\*\*PASS  
TEST 122815 SQPG LCD TTB PARITY GENERATOR & PARITY ERROR CHECK  
TEST 122815 RESULT ----- 20:28:49 --> \*\*\*PASS  
TEST 124000 SQPG DFM MODE CHECK1  
TEST 124000 RESULT ----- 20:28:49 --> \*\*\*PASS  
TEST 124010 SQPG DFM MODE CHECK2  
TEST 124010 RESULT ----- 20:28:49 --> \*\*\*PASS  
TEST 124020 SQPG DFM LOOP COUNT CHECK  
TEST 124020 RESULT ----- 20:28:49 --> \*\*\*PASS  
TEST 124030 SQPG DFM TTB CONTROL SIG CHECK  
TEST 124030 RESULT ----- 20:28:49 --> \*\*\*PASS

TEST 125000 SQPG TTB PARALLEL REGISTER READ/WRITE CHECK  
TEST 125000 RESULT ----- 20:28:57 --> \*\*\*PASS  
TEST 125005 SQPG LCD TTB PARALLEL REGISTER READ/WRITE CHECK  
TEST 125005 RESULT ----- 20:28:59 --> \*\*\*PASS  
TEST 125010 SQPG TTB PARALLEL TRANSFER CHECK  
TEST 125010 RESULT ----- 20:29:01 --> \*\*\*PASS  
TEST 125015 SQPG LCD TTB PARALLEL TRANSFER CHECK  
TEST 125015 RESULT ----- 20:29:02 --> \*\*\*PASS  
TEST 125100 SQPG TTB PARTIAL DUT REGISTER READ/WRITE CHECK  
TEST 125100 RESULT ----- 20:29:06 --> \*\*\*PASS  
TEST 125105 SQPG LCD TTB PARTIAL DUT REGISTER READ/WRITE CHECK  
TEST 125105 RESULT ----- 20:30:06 --> \*\*\*PASS  
TEST 125200 SQPG CTB MOVE CHECK  
TEST 125200 RESULT ----- 20:31:18 --> \*\*\*PASS  
TEST 125210 SQPG TTB MOVE CHECK  
TEST 125210 RESULT ----- 20:32:36 --> \*\*\*PASS  
TEST 125215 SQPG LCD TTB MOVE CHECK  
TEST 125215 RESULT ----- 20:33:51 --> \*\*\*PASS  
TEST 125220 SQPG CTB MEM INIT CHECK  
TEST 125220 RESULT ----- 20:33:51 --> \*\*\*PASS  
TEST 125230 SQPG TTB MEM INIT CHECK  
TEST 125230 RESULT ----- 20:33:53 --> \*\*\*PASS  
TEST 125300 SQPG VGC MEMORY MARCHING CHECK  
TEST 125300 RESULT ----- 20:33:54 --> \*\*\*PASS  
TEST 125310 SQPG CTB MEMORY MARCHING CHECK  
TEST 125310 RESULT ----- 20:34:10 --> \*\*\*PASS  
TEST 125320 SQPG TTB MEMORY MARCHING CHECK  
TEST 125320 RESULT ----- 20:34:59 --> \*\*\*PASS  
TEST 125325 SQPG LCD TTB MEMORY MARCHING CHECK  
TEST 125325 RESULT ----- 20:35:38 --> \*\*\*PASS  
TEST 125400 SQPG FREE RUN CHECK  
TEST 125400 RESULT ----- 20:35:38 --> \*\*\*PASS  
TEST 125410 SQPG HRESO CHECK  
TEST 125410 RESULT ----- 20:35:38 --> \*\*\*PASS  
TEST 130000 FPU REGISTER READ/WRITE 1 CHECK (FPIF)  
TEST 130000 RESULT ----- 20:36:00 --> \*\*\*PASS

TEST 130100 FPU REGISTER READ/WRITE 2 CHECK (FP/FPIF)  
TEST 130100 RESULT ----- 20:37:15 --> \*\*\*PASS  
TEST 130200 FPU REGISTER READ/WRITE 3 CHECK (PARALLEL)  
TEST 130200 RESULT ----- 20:37:17 --> \*\*\*PASS  
TEST 130250 FPU REGISTER READ/WRITE 4 CHECK (32pin PARALLEL)  
TEST 130250 RESULT ----- 20:37:18 --> \*\*\*PASS  
TEST 130300 FPU COUNTER CHECK  
TEST 130300 RESULT ----- 20:37:27 --> \*\*\*PASS  
TEST 130350 FPU TEMPERATURE UNIT DAC ACTION CHECK  
FPU initialization data successfully recovered.  
TEST 130350 RESULT ----- 20:37:45 --> \*\*\*PASS  
TEST 137000 TRG REGISTER READ/WRITE CHECK  
TEST 137000 RESULT ----- 20:37:48 --> \*\*\*PASS  
TEST 137300 TRG COUNTER CHECK  
TEST 137300 RESULT ----- 20:37:53 --> \*\*\*PASS  
TEST 130500 FPU INPUT CHECK  
FPU initialization data successfully recovered.  
TEST 130500 RESULT ----- 20:38:10 --> \*\*\*PASS  
TEST 130600 FPU LINEARITY CHECK (PTG)  
FPU initialization data successfully recovered.  
TEST 130600 RESULT ----- 20:39:26 --> \*\*\*PASS  
TEST 130700 FPU MUTUAL COMPARE CHECK  
TEST 130700 RESULT ----- 20:39:37 --> \*\*\*PASS  
TEST 130800 FPU FORMAT CONTROL CHECK  
FPU initialization data successfully recovered.  
TEST 130800 RESULT ----- 20:40:01 --> \*\*\*PASS  
TEST 130900 FPU DIGITAL COMPARE CHECK  
FPU initialization data successfully recovered.  
TEST 130900 RESULT ----- 20:40:32 --> \*\*\*PASS  
TEST 137500 TRG INPUT CHECK  
SQPG initialization data successfully recovered.  
TRIGFP initialization data successfully recovered.  
TEST 137500 RESULT ----- 20:40:48 --> \*\*\*PASS  
TEST 137600 TRG LINEARITY CHECK  
TRIGFP initialization data successfully recovered.  
TEST 137600 RESULT ----- 20:41:13 --> \*\*\*PASS

TEST 137700 TRG MUTUAL COMPARE CHECK  
TEST 137700 RESULT ----- 20:41:15 --> \*\*\*PASS  
TEST 137800 TRG FORMAT CONTROL CHECK  
TRIGFP            initialization data successfully recovered.  
TEST 137800 RESULT ----- 20:41:23 --> \*\*\*PASS  
TEST 137900 TRG DIGITAL COMPARE CHECK  
TRIGFP            initialization data successfully recovered.  
TEST 137900 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140100 TH1 STATION SELECT REGISTER RESET CHECK  
TEST 140100 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140105 TH1 STATION SELECT REGISTER SYSTEM RESET CHECK  
TEST 140105 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140110 TH1 PIN DOMAIN REGISTER RESET CHECK  
TEST 140110 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140115 TH1 PIN DOMAIN REGISTER SYSTEM RESET CHECK  
TEST 140115 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140120 TH1 CONT REGISTER RESET CHECK  
TEST 140120 RESULT ----- 20:41:30 --> \*\*\*PASS  
TEST 140125 TH1 CONT REGISTER SYSTEM RESET CHECK  
TEST 140125 RESULT ----- 20:41:31 --> \*\*\*PASS  
TEST 140150 TH1 DC PARA RESET CHECK  
TEST 140150 RESULT ----- 20:41:31 --> \*\*\*PASS  
TEST 140200 TH1 RON/ROF REGISTER READ/WRITE CHECK  
TEST 140200 RESULT ----- 20:41:31 --> \*\*\*PASS  
TEST 140300 TH1 PIN/CONT REGISTER READ/WRITE CHECK  
TEST 140300 RESULT ----- 20:41:31 --> \*\*\*PASS  
TEST 140310 TH1 OFFSET & GAIN REGISTER READ/WRITE CHECK  
TEST 140310 RESULT ----- 20:41:32 --> \*\*\*PASS  
TEST 140500 TH1 RON/ROFF TIMER OPERATION TIME CHECK  
TEST 140500 RESULT ----- 20:41:40 --> \*\*\*PASS  
TEST 140510 TH1 RON/ROFF TIMER OPERATION RON/ROFF SET CHECK  
TEST 140510 RESULT ----- 20:41:40 --> \*\*\*PASS  
TEST 140520 TH1 DIRECT RON OPERATION RON/ROFF SET CHECK  
TEST 140520 RESULT ----- 20:41:41 --> \*\*\*PASS  
TEST 140530 TH1 SETTLING BUSY FLAG OPERATION CHECK  
TEST 140530 RESULT ----- 20:41:45 --> \*\*\*PASS

TEST 140540 TH1 SETTling BUSY FLAG OPERATION2 CHECK  
TEST 140540 RESULT ----- 20:42:02 --> \*\*\*PASS  
TEST 140600 TH1 PIN GROUP SETUP OPERATION CHECK  
TEST 140600 RESULT ----- 20:42:02 --> \*\*\*PASS  
TEST 140610 TH1 PIN PARALLEL MODE READ/WRITE CHECK  
TEST 140610 RESULT ----- 20:42:10 --> \*\*\*PASS  
TEST 140650 TH1 VT FUNCTION/EXTRA REGISTER CHECK  
TEST 140650 RESULT ----- 20:42:10 --> \*\*\*PASS  
TEST 140700 TH1 TERM M2R5V SENSE CHECK  
TEST 140700 RESULT ----- 20:42:10 --> \*\*\*PASS  
TEST 140800 TH1 FCSTOP LINE CHECK  
SQPG            initialization data successfully recovered.  
TEST 140800 RESULT ----- 20:42:11 --> \*\*\*PASS  
TEST 140900 TH1 INIT TH ADJUSTMENT CHECK  
TEST 140900 RESULT ----- 20:44:54 --> \*\*\*PASS  
TEST 141100 TH1 DR OUTPUT VOLTAGE LINEARITY & RON/ROF CHECK  
TEST 141100 RESULT ----- 20:45:09 --> \*\*\*PASS  
TEST 141110 TH1 DR OUTPUT CURRENT & IMPEDANCE CHECK  
TEST 141110 RESULT ----- 20:45:18 --> \*\*\*PASS  
TEST 141120 TH1 DR OUTPUT CURRENT LIMIT CHECK  
TEST 141120 RESULT ----- 20:45:22 --> \*\*\*PASS  
TEST 141200 TH1 VT LINEARITY VOLTAGE & RON/ROF CHECK  
TEST 141200 RESULT ----- 20:45:28 --> \*\*\*PASS  
TEST 141210 TH1 VT CURRENT & RESISTANCE CHECK  
TEST 141210 RESULT ----- 20:45:39 --> \*\*\*PASS  
TEST 141300 TH1 PL CURRENT LINEARITY VOLTAGE & RON/ROF CHECK  
TEST 141300 RESULT ----- 20:46:03 --> \*\*\*PASS  
TEST 141310 TH1 PL THRESHOLD VOLTAGE CHECK  
TEST 141310 RESULT ----- 20:46:07 --> \*\*\*PASS  
TEST 141320 TH1 PL VT VOLTAGE CHECK  
TEST 141320 RESULT ----- 20:46:23 --> \*\*\*PASS  
TEST 141400 TH1 LIMITER FAIL SENSE VOLTAGE CHECK  
TEST 141400 RESULT ----- 20:46:53 --> \*\*\*PASS  
TEST 141500 TH1 LIMITER FAIL MASK OPERATION CHECK  
TEST 141500 RESULT ----- 20:47:27 --> \*\*\*PASS  
TEST 141600 TH1 RELAY OFF LEAK CURRENT CHECK

TEST 141600 RESULT ----- 20:47:35 --> \*\*\*PASS  
TEST 142000 TH1 I/O LEAK CURRENT CHECK  
TEST 142000 RESULT ----- 20:47:42 --> \*\*\*PASS  
TEST 142100 TH1 CP(HiZ) REFERENCE VOLTAGE LINEARITY CHECK  
TEST 142100 RESULT ----- 20:49:12 --> \*\*\*PASS  
TEST 142110 TH1 CP(VT) REFERENCE VOLTAGE LINEARITY CHECK  
TEST 142110 RESULT ----- 20:51:06 --> \*\*\*PASS  
TEST 142200 TH1 DCLMP VOLTAGE LINEARITY & RON/ROF CHECK  
TEST 142200 RESULT ----- 20:51:22 --> \*\*\*PASS  
TEST 142210 TH1 DCLMP CURRENT LIMIT CHECK  
TEST 142210 RESULT ----- 20:51:26 --> \*\*\*PASS  
TEST 144000 TH1 PRE DR - CP PHASE CHECK  
TEST 144000 RESULT ----- 20:51:28 --> \*\*\*PASS  
TEST 144100 TH1 PRE I/O TIMING (NORMAL MODE) CHECK  
TEST 144100 RESULT ----- 20:51:33 --> \*\*\*PASS  
TEST 144200 TH1 PRE DRE MINIMUM ON/OFF (NORMAL MODE) CHECK  
TEST 144200 RESULT ----- 20:51:42 --> \*\*\*PASS  
TEST 144500 TH1 DRIVER/COMPARETER TR/TF CHECK  
TEST 144500 RESULT ----- 20:52:02 --> \*\*\*PASS  
TEST 145000 TH1 DR - CP PHASE CHECK  
TEST 145000 RESULT ----- 20:52:05 --> \*\*\*PASS  
TEST 145100 TH1 I/O TIMING (NORMAL MODE) CHECK  
TEST 145100 RESULT ----- 20:52:10 --> \*\*\*PASS  
TEST 145120 TH1 I/O TIMING (VTT MODE) CHECK  
TEST 145120 RESULT ----- 20:52:15 --> \*\*\*PASS  
TEST 145200 TH1 DRE MINIMUM ON/OFF (NORMAL MODE) CHECK  
TEST 145200 RESULT ----- 20:52:24 --> \*\*\*PASS  
TEST 145220 TH1 DRE MINIMUM ON/OFF (VTT MODE) CHECK  
TEST 145220 RESULT ----- 20:52:33 --> \*\*\*PASS  
TEST 140910 TH1 INIT TRIGTH ADJUSTMENT CHECK  
TRIGFP            initialization data successfully recovered.  
TEST 140910 RESULT ----- 20:52:51 --> \*\*\*PASS  
TEST 143000 TH1 TRIGGER DR OUTPUT VOLTAGE LINEARITY CHECK  
TEST 143000 RESULT ----- 20:52:57 --> \*\*\*PASS  
TEST 143010 TH1 TRIGGER DR OUTPUT CURRENT & IMPEDANCE CHECK  
TEST 143010 RESULT ----- 20:53:02 --> \*\*\*PASS

TEST 143100 TH1 TRIGGER CP REFERENCE VOLTAGE LINEARITY CHECK  
TEST 143100 RESULT ----- 20:53:10 --> \*\*\*PASS  
TEST 143110 TH1 TRIGGER CP REFERENCE VOLTAGE HYSTERESIS CHECK  
TEST 143110 RESULT ----- 20:53:17 --> \*\*\*PASS  
TEST 150100 FPU AFTER TH1 FUNCTION CHECK  
TRIGFPTH        initialization data successfully recovered.  
TEST 150100 RESULT ----- 20:53:47 --> \*\*\*PASS  
TEST 157100 TRG AFTER TH1 FUNCTION CHECK  
FPU            initialization data successfully recovered.  
TRIGFPTH        initialization data successfully recovered.  
TEST 157100 RESULT ----- 20:54:09 --> \*\*\*PASS  
TEST 160000 SQPG DFM FAIL PATH CHECK  
TEST 160000 RESULT ----- 20:54:17 --> \*\*\*PASS  
TEST 160002 SQPG HSIF DFM FAIL PATH CHECK  
TEST 160002 RESULT ----- 20:54:17 --> \*\*\*PASS  
TEST 160005 SQPG LCD DFM FAIL PATH CHECK  
TEST 160005 RESULT ----- 20:54:18 --> \*\*\*PASS  
TEST 160010 SQPG DFM TOFL PATH CHECK  
TEST 160010 RESULT ----- 20:54:19 --> \*\*\*PASS  
TEST 160015 SQPG LCD DFM TOFL PATH CHECK  
TEST 160015 RESULT ----- 20:54:19 --> \*\*\*PASS  
TEST 160020 SQPG DFM STORE PATH CHECK  
TEST 160020 RESULT ----- 20:54:19 --> \*\*\*PASS  
TEST 160022 SQPG HSIF DFM STORE PATH CHECK  
TEST 160022 RESULT ----- 20:54:20 --> \*\*\*PASS  
TEST 160025 SQPG LCD DFM STORE PATH CHECK  
TEST 160025 RESULT ----- 20:54:20 --> \*\*\*PASS  
TEST 160030 SQPG DFM FULL STORE CHECK  
TEST 160030 RESULT ----- 20:54:21 --> \*\*\*PASS  
TEST 160500 SQPG HMATCH FLAGH PATH CHECK  
TEST 160500 RESULT ----- 20:54:22 --> \*\*\*PASS  
TEST 160600 SQPG LMATCH FLAGL PATH CHECK  
TEST 160600 RESULT ----- 20:54:23 --> \*\*\*PASS  
TEST 160605 SQPG LCD LMATCH FLAGL PATH CHECK  
TEST 160605 RESULT ----- 20:54:23 --> \*\*\*PASS  
TEST 161000 SQPG DFM BOUNDARY CHECK 1

TEST 161000 RESULT ----- 20:54:24 --> \*\*\*PASS  
TEST 161010 SQPG DFM BOUNDARY CHECK 2  
TEST 161010 RESULT ----- 20:54:24 --> \*\*\*PASS  
TEST 161020 SQPG DFM BOUNDARY CHECK 3  
TEST 161020 RESULT ----- 20:54:24 --> \*\*\*PASS  
TEST 161030 SQPG DFM DONE FLAG MODE CHECK  
TEST 161030 RESULT ----- 20:54:24 --> \*\*\*PASS  
TEST 161100 SQPG DFM FAIL STORE CHECK 1  
TEST 161100 RESULT ----- 20:54:24 --> \*\*\*PASS  
TEST 161110 SQPG DFM FAIL STORE CHECK 2  
TEST 161110 RESULT ----- 20:54:25 --> \*\*\*PASS  
TEST 161115 SQPG LCD DFM FAIL STORE CHECK 2  
TEST 161115 RESULT ----- 20:54:25 --> \*\*\*PASS  
TEST 161200 SQPG DFM NAVIGATION CHECK 1  
TEST 161200 RESULT ----- 20:54:26 --> \*\*\*PASS  
TEST 161210 SQPG DFM NAVIGATION CHECK 2  
TEST 161210 RESULT ----- 20:54:26 --> \*\*\*PASS  
TEST 161215 SQPG LCD DFM NAVIGATION CHECK 2  
TEST 161215 RESULT ----- 20:54:27 --> \*\*\*PASS  
TEST 161500 SQPG DFM TOFL PARALLEL CHECK  
TEST 161500 RESULT ----- 20:54:28 --> \*\*\*PASS  
TEST 161505 SQPG LCD DFM TOFL PARALLEL CHECK  
TEST 161505 RESULT ----- 20:54:28 --> \*\*\*PASS  
TEST 161510 SQPG DFM TOFL PARALLEL AND FAIL CHECK  
TEST 161510 RESULT ----- 20:54:28 --> \*\*\*PASS  
TEST 161520 SQPG DFM TOFL PARALLEL OR FAIL CHECK  
TEST 161520 RESULT ----- 20:54:29 --> \*\*\*PASS  
TEST 161530 SQPG DFM TOFL PARALLEL FIRST FAIL CHECK  
TEST 161530 RESULT ----- 20:54:29 --> \*\*\*PASS  
TEST 162000 SQPG HMATCH FUNCTION CHECK 1  
TEST 162000 RESULT ----- 20:54:30 --> \*\*\*PASS  
TEST 162010 SQPG HMATCH FUNCTION CHECK 2  
TEST 162010 RESULT ----- 20:54:30 --> \*\*\*PASS  
TEST 162020 SQPG HMATCH PULSE TRAIN CHECK 1  
TEST 162020 RESULT ----- 20:54:37 --> \*\*\*PASS  
TEST 162021 SQPG HMATCH PULSE TRAIN CHECK 2

TEST 162021 RESULT ----- 20:54:43 --> \*\*\*PASS  
TEST 162100 SQPG LMATCH FUNCTION CHECK 1  
TEST 162100 RESULT ----- 20:54:43 --> \*\*\*PASS  
TEST 162105 SQPG LCD LMATCH FUNCTION CHECK 1  
TEST 162105 RESULT ----- 20:54:44 --> \*\*\*PASS  
TEST 162110 SQPG LMATCH FUNCTION CHECK 2  
TEST 162110 RESULT ----- 20:54:44 --> \*\*\*PASS  
TEST 162120 SQPG LMATCH FUNCTION CHECK 3  
TEST 162120 RESULT ----- 20:54:45 --> \*\*\*PASS  
TEST 162200 SQPG LMATCH PULSE TRAIN CHECK 1  
TEST 162200 RESULT ----- 20:54:51 --> \*\*\*PASS  
TEST 162210 SQPG LMATCH PULSE TRAIN CHECK 2  
TEST 162210 RESULT ----- 20:54:57 --> \*\*\*PASS  
TEST 162500 SQPG MATCH DUT REJECT CHECK 1  
TEST 162500 RESULT ----- 20:54:58 --> \*\*\*PASS  
TEST 162510 SQPG MATCH DUT REJECT CHECK 2  
TEST 162510 RESULT ----- 20:54:59 --> \*\*\*PASS  
TEST 162515 SQPG LCD FLAGL PARALLEL CHECK  
TEST 162515 RESULT ----- 20:55:00 --> \*\*\*PASS  
TEST 162800 SQPG MATCH RATE ERROR CHECK  
TEST 162800 RESULT ----- 20:55:01 --> \*\*\*PASS  
TEST 163000 SQPG LCD DC FUNCTION CHECK  
TEST 163000 RESULT ----- 20:55:01 --> \*\*\*PASS  
TEST 163010 SQPG LCD DC ENABLE FUNCTION CHECK  
TEST 163010 RESULT ----- 20:55:02 --> \*\*\*PASS  
TEST 163020 SQPG LCD DC MASTER MASK FUNCTION CHECK  
TEST 163020 RESULT ----- 20:55:02 --> \*\*\*PASS  
TEST 163030 SQPG LCD DC CPE ENABLE FUNCTION CHECK  
TEST 163030 RESULT ----- 20:55:03 --> \*\*\*PASS  
TEST 163040 SQPG LCD DC LA MODE FUNCTION CHECK  
TEST 163040 RESULT ----- 20:55:03 --> \*\*\*PASS  
TEST 165100 SQPG DFM PARTIAL DUT READ CHECK  
TEST 165100 RESULT ----- 20:55:04 --> \*\*\*PASS  
TEST 165105 SQPG LCD DFM PARTIAL DUT READ CHECK  
TEST 165105 RESULT ----- 20:55:05 --> \*\*\*PASS  
TEST 166100 SQPG WAIT OR FAIL CHECK

TEST 166100 RESULT ----- 20:55:07 --> \*\*\*PASS  
TEST 180110 AQM REGISTER W/R CHECK  
TEST 180110 RESULT ----- 20:55:07 --> \*\*\*PASS  
TEST 180130 AQM ACQUISITION MEMORY W/R CHECK  
TEST 180130 RESULT ----- 20:55:19 --> \*\*\*PASS  
TEST 180140 AQM SCATTER GATHER DMA CHECK  
TEST 180140 RESULT ----- 20:55:21 --> \*\*\*PASS  
TEST 180200 AQM STATUS CHECK  
TEST 180200 RESULT ----- 20:55:34 --> \*\*\*PASS  
TEST 180210 AQM TIME OUT CHECK  
TEST 180210 RESULT ----- 20:57:34 --> \*\*\*PASS  
TEST 180220 AQM ACQUISITION MODE CHECK  
TEST 180220 RESULT ----- 20:57:34 --> \*\*\*PASS  
TEST 180230 AQM STEP COUNT CHECK  
TEST 180230 RESULT ----- 21:00:01 --> \*\*\*PASS  
TEST 180240 AQM MUX COUNT CHECK  
TEST 180240 RESULT ----- 21:00:04 --> \*\*\*PASS  
TEST 180250 AQM AVERAGE COUNT CHECK  
TEST 180250 RESULT ----- 21:01:25 --> \*\*\*PASS  
TEST 180260 AQM ACQUISITION ENABLE CHECK  
TEST 180260 RESULT ----- 21:01:29 --> \*\*\*PASS  
TEST 180300 AQM TAG DATA MEMORY W/R CHECK  
TEST 180300 RESULT ----- 21:01:30 --> \*\*\*PASS  
TEST 180310 AQM CALC RESULT MEMORY W/R CHECK  
TEST 180310 RESULT ----- 21:01:45 --> \*\*\*PASS  
TEST 180340 AQM INSTRUCTION MEMORY W/R CHECK  
TEST 180340 RESULT ----- 21:01:54 --> \*\*\*PASS  
TEST 180350 AQM ACQUISITION MEMORY DIAG CHECK  
TEST 180350 RESULT ----- 21:01:55 --> \*\*\*PASS  
TEST 180360 AQM CALCULATOR MEMORY DIAG CHECK  
TEST 180360 RESULT ----- 21:01:58 --> \*\*\*PASS  
TEST 180370 AQM LOCAL RAM W/R CHECK  
TEST 180370 RESULT ----- 21:01:59 --> \*\*\*PASS  
TEST 180380 AQM\_CALC\_TIMEOUT CHECK  
TEST 180380 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180400 AQM MCU REGISTER(0-15) W/R CHECK

TEST 180400 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180410 AQM RPOGRAM COUNTER CHECK  
TEST 180410 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180420 AQM MCU INSTRUCTION CHECK  
TEST 180420 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180430 AQM MCU BUS REGISTER W/R CHECK  
TEST 180430 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180440 AQM MCU DRAM W/R CHECK  
TEST 180440 RESULT ----- 21:02:00 --> \*\*\*PASS  
TEST 180450 AQM WORK MEMORY W/R CHECK  
TEST 180450 RESULT ----- 21:02:02 --> \*\*\*PASS  
TEST 180460 AQM XBUS DATA TRANSFER CHECK  
TEST 180460 RESULT ----- 21:02:59 --> \*\*\*PASS  
TEST 180470 AQM PCU CHECK  
TEST 180470 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 180520 AQM MCU INTERRUPT CHECK  
TEST 180520 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 180530 AQM MCU STATUS CHECK  
TEST 180530 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 180550 AQM MCU CONTROL CHECK  
TEST 180550 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 180560 AQM MCU BREAK POINT CHECK  
TEST 180560 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 180580 AQM TIMER CHECK  
TEST 180580 RESULT ----- 21:03:04 --> \*\*\*PASS  
TEST 181010 EVENT NORMAL REGISTER W/R CHECK  
TEST 181010 RESULT ----- 21:03:05 --> \*\*\*PASS  
TEST 181020 EVENT NORMAL REGISTER RESET CHECK  
TEST 181020 RESULT ----- 21:03:05 --> \*\*\*PASS  
TEST 181030 EVENT REGISTER W/R CHECK (CHECK BUSY)  
TEST 181030 RESULT ----- 21:03:05 --> \*\*\*PASS  
TEST 181040 EVENT REGISTER RESET CHECK (CHECK BUSY)  
TEST 181040 RESULT ----- 21:03:08 --> \*\*\*PASS  
TEST 181050 EVENT CAL CONT REGISTER W/R CHECK  
TEST 181050 RESULT ----- 21:03:08 --> \*\*\*PASS  
TEST 181060 EVENT REGISTER SETTLING BUSY TIME CHECK

TEST 181060 RESULT ----- 21:03:08 --> \*\*\*PASS  
TEST 181070 EVENT ADC CONTROL LINE CHECK  
TEST 181070 RESULT ----- 21:03:08 --> \*\*\*PASS  
TEST 181080 EVENT ADC AUTO SAMPLING COUNTER CHECK  
TEST 181080 RESULT ----- 21:03:09 --> \*\*\*PASS  
TEST 181090 EVENT CAL REFERENCE VOLTAGE CHECK  
TEST 181090 RESULT ----- 21:03:10 --> \*\*\*PASS  
TEST 181100 EVENT CAL LINE CONNECTION CHECK  
TEST 181100 RESULT ----- 21:03:11 --> \*\*\*PASS  
TEST 181110 EVENT LCD OFFSET VOLTAGE CHECK  
TEST 181110 RESULT ----- 21:03:11 --> \*\*\*PASS  
TEST 181510 EVENT GREF REGISTER W/R CHECK  
TEST 181510 RESULT ----- 21:03:11 --> \*\*\*PASS  
TEST 181520 EVENT GREF REGISTER RESET CHECK  
TEST 181520 RESULT ----- 21:03:16 --> \*\*\*PASS  
TEST 181530 EVENT GREF ADRS/DATA LINE CHECK  
TEST 181530 RESULT ----- 21:03:17 --> \*\*\*PASS  
TEST 181540 EVENT GREF MEMORY W/R CHECK  
TEST 181540 RESULT ----- 21:03:38 --> \*\*\*PASS  
TEST 181550 EVENT GREF GINC LINE CHECK  
TEST 181550 RESULT ----- 21:03:38 --> \*\*\*PASS  
TEST 181560 EVENT GREF CAL LINE CHECK  
TEST 181560 RESULT ----- 21:03:39 --> \*\*\*PASS  
TEST 181570 EVENT GREF INIT CHECK  
TEST 181570 RESULT ----- 21:04:18 --> \*\*\*PASS  
TEST 181580 EVENT GREF DC ACCURACY CHECK  
TEST 181580 RESULT ----- 21:04:46 --> \*\*\*PASS  
TEST 181600 EVENT GREF GINC START/STOP CHECK  
TEST 181600 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 181610 EVENT GREF SERIAL DATA CHECK  
TEST 181610 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 186000 RVS MOUNT CHECK  
TEST 186000 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 186110 RVS PIN DOMAIN REGISTER RESET CHECK  
TEST 186110 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 186115 RVS PIN DOMAIN REGISTER SYSTEM RESET CHECK

TEST 186115 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 186200 RVS RON/ROF REGISTER READ/WRITE CHECK  
TEST 186200 RESULT ----- 21:04:50 --> \*\*\*PASS  
TEST 186300 RVS RVS CONT-FPGA REGISTER READ/WRITE CHECK  
TEST 186300 RESULT ----- 21:04:57 --> \*\*\*PASS  
TEST 186500 RVS RON/ROF TIMER OPERATION TIME CHECK  
TEST 186500 RESULT ----- 21:05:03 --> \*\*\*PASS  
TEST 186530 RVS BUSY FLAG OPERATION CHECK( EVENT READ )  
TEST 186530 RESULT ----- 21:05:06 --> \*\*\*PASS  
TEST 186540 RVS PARALLEL TEST CONDITION CHECK  
TEST 186540 RESULT ----- 21:05:06 --> \*\*\*PASS  
TEST 186550 RVS LIMITER FAIL LINE CHECK  
TEST 186550 RESULT ----- 21:05:07 --> \*\*\*PASS  
TEST 186560 RVS TOTAL DC / DUT MASK CHECK  
TEST 186560 RESULT ----- 21:05:08 --> \*\*\*PASS  
TEST 186900 RVS MEASURE REFERENCE RESISTORS  
TEST 186900 RESULT ----- 21:05:10 --> \*\*\*PASS  
TEST 186910 RVS REFERENCE VOLTAGE INITIALIZE  
TEST 186910 RESULT ----- 21:05:14 --> \*\*\*PASS  
TEST 186920 RVS VS SUB INITIALIZE  
TEST 186920 RESULT ----- 21:06:06 --> \*\*\*PASS  
TEST 186930 RVS IM SUB INITIALIZE  
TEST 186930 RESULT ----- 21:06:19 --> \*\*\*PASS  
TEST 186940 RVS VM SUB INITIALIZE  
TEST 186940 RESULT ----- 21:06:20 --> \*\*\*PASS  
TEST 186950 RVS CURRENT CLAMP SUB INITIALIZE  
TEST 186950 RESULT ----- 21:06:23 --> \*\*\*PASS  
TEST 186955 RVS SUB DVM CALIBRATION  
TEST 186955 RESULT ----- 21:06:48 --> \*\*\*PASS  
TEST 186960 RVS VS PARALLEL INITIALIZE  
TEST 186960 RESULT ----- 21:26:15 --> \*\*\*PASS  
TEST 186970 RVS IM PARALLEL INITIALIZE  
TEST 186970 RESULT ----- 21:27:11 --> \*\*\*PASS  
TEST 186980 RVS VM INITIALIZE  
TEST 186980 RESULT ----- 21:27:57 --> \*\*\*PASS  
TEST 186990 RVS CURRENT CLAMP INITIALIZE

TEST 186990 RESULT ----- 21:29:12 --> \*\*\*PASS  
TEST 188000 RVS PB CONNECTION CHECK  
TEST 188000 RESULT ----- 21:29:20 --> \*\*\*PASS  
TEST 183100 LCD DCM RESET CHECK  
TEST 183100 RESULT ----- 21:29:22 --> \*\*\*PASS  
TEST 183110 LCD PIN DOMAIN REGISTER RESET CHECK  
TEST 183110 RESULT ----- 21:29:33 --> \*\*\*PASS  
TEST 183115 LCD PIN DOMAIN REGISTER SYSTEM RESET CHECK  
TEST 183115 RESULT ----- 21:29:45 --> \*\*\*PASS  
TEST 183120 LCD PIN CONT REGISTER RESET CHECK  
TEST 183120 RESULT ----- 21:29:45 --> \*\*\*PASS  
TEST 183125 LCD PIN CONT REGISTER SYSTEM RESET CHECK  
TEST 183125 RESULT ----- 21:29:45 --> \*\*\*PASS  
TEST 183150 LCD PIN DC PARA RESET CHECK  
TEST 183150 RESULT ----- 21:29:45 --> \*\*\*PASS  
TEST 183300 LCD PIN/CONT REGISTER READ/WRITE CHECK  
TEST 183300 RESULT ----- 21:30:07 --> \*\*\*PASS  
TEST 183310 LCD OFFSET/GAIN REGISTER READ/WRITE CHECK  
TEST 183310 RESULT ----- 21:30:17 --> \*\*\*PASS  
TEST 183540 LCD FIFO BUFFER CHECK  
TEST 183540 RESULT ----- 21:30:30 --> \*\*\*PASS  
TEST 183600 LCD PIN GROUP SETUP OPERATION CHECK  
TEST 183600 RESULT ----- 21:30:33 --> \*\*\*PASS  
TEST 183610 LCD PIN PARALLEL MODE READ/WRITE CHECK  
TEST 183610 RESULT ----- 21:31:15 --> \*\*\*PASS  
TEST 183710 PPDC REGISTER RESET CHECK  
TEST 183710 RESULT ----- 21:31:21 --> \*\*\*PASS  
TEST 183715 PPDC REGISTER SYSTEM RESET CHECK  
TEST 183715 RESULT ----- 21:31:27 --> \*\*\*PASS  
TEST 183750 PIN DC PARA2 RESET CHECK  
TEST 183750 RESULT ----- 21:31:28 --> \*\*\*PASS  
TEST 183800 PPDC PIN/CONT REGISTER READ/WRITE CHECK  
TEST 183800 RESULT ----- 21:31:47 --> \*\*\*PASS  
TEST 183820 PPDC PIN GROUP SETUP OPERATION CHECK  
TEST 183820 RESULT ----- 21:31:47 --> \*\*\*PASS  
TEST 183830 PPDC PIN PARALLEL MODE READ/WRITE CHECK

TEST 183830 RESULT ----- 21:31:57 --> \*\*\*PASS  
TEST 183900 LCD INIT LCD ADJUSTMENT CHECK  
TEST 183900 RESULT ----- 22:01:43 --> \*\*\*PASS  
TEST 184060 LCD LIMITER FAIL SENSE VOLTAGE CHECK  
TEST 184060 RESULT ----- 22:02:02 --> \*\*\*PASS  
TEST 184130 LCD PL CURRENT LINEARITY VOLTAGE & RON/ROF CHECK  
TEST 184130 RESULT ----- 22:02:54 --> \*\*\*PASS  
TEST 184150 LCD PL VT VOLTAGE CHECK  
TEST 184150 RESULT ----- 22:06:25 --> \*\*\*PASS  
TEST 184200 LCD COMP LINEARITY VOLTAGE CHECK  
TEST 184200 RESULT ----- 22:07:45 --> \*\*\*PASS  
TEST 184500 LCD TMU FUNCTION CHECK  
TEST 184500 RESULT ----- 22:07:47 --> \*\*\*PASS  
TEST 185000 LCD DGT SIGNAL LINE CHECK  
TEST 185000 RESULT ----- 22:07:48 --> \*\*\*PASS  
TEST 185010 LCD AS OFFSET CHECK  
TEST 185010 RESULT ----- 22:07:55 --> \*\*\*PASS  
TEST 185020 LCD DGT OVER RANGE DETECT CHECK  
TEST 185020 RESULT ----- 22:08:13 --> \*\*\*PASS  
TEST 185100 LCD DGT GUARANTEE CHECK  
TEST 185100 RESULT ----- 22:10:23 --> \*\*\*PASS  
TEST 185140 LCD DGT DIFFERENTIAL GUARANTEE CHECK  
TEST 185140 RESULT ----- 22:11:12 --> \*\*\*PASS  
TEST 185160 LCD DGT CMV GUARANTEE CHECK  
TEST 185160 RESULT ----- 22:15:50 --> \*\*\*PASS  
TEST 185200 LCD DGT GREF MUX CHECK  
TEST 185200 RESULT ----- 22:15:54 --> \*\*\*PASS  
TEST 185220 LCD DGT GREF FUNCTION CHECK  
TEST 185220 RESULT ----- 22:16:23 --> \*\*\*PASS  
TEST 185240 LCD DGT GREF LPF CHECK  
TEST 185240 RESULT ----- 22:16:32 --> \*\*\*PASS  
TEST 185300 LCD DGT REALTIME CHECK  
TEST 185300 RESULT ----- 22:16:38 --> \*\*\*PASS  
TEST 185340 LCD DGT SETTLING CHECK  
TEST 185340 RESULT ----- 22:16:46 --> \*\*\*PASS  
TEST 185430 LCD DGT PIN\_INC MODE CHECK

TEST 185430 RESULT ----- 22:16:48 --> \*\*\*PASS  
TEST 185440 LCD DGT STEP\_INC MODE CHECK  
TEST 185440 RESULT ----- 22:16:49 --> \*\*\*PASS  
TEST 185450 LCD DGT GREF REALTIME CHECK (NORMAL)  
TEST 185450 RESULT ----- 22:17:40 --> \*\*\*PASS  
TEST 185460 LCD DGT GREF REALTIME CHECK (DIFFERNCE)  
TEST 185460 RESULT ----- 22:18:43 --> \*\*\*PASS  
TEST 185600 LCD PPDC VSIM VS ACCURACY CHECK  
TEST 185600 RESULT ----- 22:18:44 --> \*\*\*PASS  
TEST 185620 LCD PPDC VSIM IM ACCURACY CHECK  
TEST 185620 RESULT ----- 22:20:33 --> \*\*\*PASS  
TEST 185640 LCD PPDC VSIM IM-CLAMP CHECK  
TEST 185640 RESULT ----- 22:21:05 --> \*\*\*PASS  
TEST 185680 LCD PPDC ISVM IS ACCURACY CHECK  
TEST 185680 RESULT ----- 22:22:06 --> \*\*\*PASS  
TEST 185700 LCD PPDC ISVM VM ACCURACY CHECK  
TEST 185700 RESULT ----- 22:22:20 --> \*\*\*PASS  
TEST 185710 LCD PPDC ISVM VM ACCURACY CHECK2  
TEST 185710 RESULT ----- 22:22:59 --> \*\*\*PASS  
TEST 185720 LCD PPDC ISVM VM-CLAMP CHECK  
TEST 185720 RESULT ----- 22:23:00 --> \*\*\*PASS  
TEST 185760 LCD PPDC PARALLEL FUNCTION CHECK  
TEST 185760 RESULT ----- 22:23:59 --> \*\*\*PASS  
TEST 185780 LCD PPDC VSIM IM SETTLING CHECK  
TEST 185780 RESULT ----- 22:24:03 --> \*\*\*PASS  
TEST 185800 LCD ON RESISTANCE CHECK  
TEST 185800 RESULT ----- 22:27:06 --> \*\*\*PASS  
TEST 185810 LCD OFF LEAK CURRENT CHECK  
TEST 185810 RESULT ----- 22:32:32 --> \*\*\*PASS  
TEST 185820 LCD MAKE TIME CHECK  
TEST 185820 RESULT ----- 22:36:02 --> \*\*\*PASS  
TEST 185830 LCD BREAK TIME CHECK  
TEST 185830 RESULT ----- 22:41:14 --> \*\*\*PASS  
TEST 190000 LIDD BOARD STATUS CHECK  
TEST 190000 RESULT ----- 22:41:15 --> \*\*\*PASS  
TEST 190010 LIDD CONT REGISTER RESET CHECK

TEST 190010 RESULT ----- 22:41:15 --> \*\*\*PASS  
TEST 190020 LIDD CONT REGISTER R/W CHECK  
TEST 190020 RESULT ----- 22:41:15 --> \*\*\*PASS  
TEST 190040 LIDD CHANNEL DOMAIN REGISTER R/W CHECK  
TEST 190040 RESULT ----- 22:41:15 --> \*\*\*PASS  
TEST 190080 LIDD MEMORY R/W CHECK  
TEST 190080 RESULT ----- 22:41:27 --> \*\*\*PASS  
TEST 190100 LIDD PARALLEL R/W CHECK  
TEST 190100 RESULT ----- 22:41:27 --> \*\*\*PASS  
TEST 190200 LIDD RELAY CONTACT CHECK  
TEST 190200 RESULT ----- 22:41:45 --> \*\*\*PASS  
TEST 190250 LIDD RELAY MASK CHECK  
TEST 190250 RESULT ----- 22:42:06 --> \*\*\*PASS  
TEST 190300 LIDD VS OUTPUT CHECK  
TEST 190300 RESULT ----- 22:42:11 --> \*\*\*PASS  
TEST 190350 LIDD IM OUTPUT CHECK  
TEST 190350 RESULT ----- 22:42:23 --> \*\*\*PASS  
TEST 190400 LIDD IM SETTling CHECK  
TEST 190400 RESULT ----- 22:42:46 --> \*\*\*PASS  
TEST 190500 LIDD INIT ADJUSTMENT CHECK  
TEST 190500 RESULT ----- 22:43:47 --> \*\*\*PASS  
TEST 190600 LIDD IM MEASUREMENT CHECK  
TEST 190600 RESULT ----- 22:44:09 --> \*\*\*PASS  
TEST 190650 LIDD VS MONITOR MEASUREMENT CHECK  
TEST 190650 RESULT ----- 22:44:34 --> \*\*\*PASS  
TEST 190700 LIDD SAMPLING TRIG CHECK  
TEST 190700 RESULT ----- 22:46:30 --> \*\*\*PASS  
TEST 193128 DPU-PG CABLE CONNECTION CHECK  
TEST 193128 RESULT ----- 22:46:30 --> \*\*\*PASS  
TEST 192000 HSIF BOARD REVISION CHECK  
TEST 192000 RESULT ----- 22:46:30 --> \*\*\*PASS  
TEST 192010 HSIF REGISTER R/W CHECK  
TEST 192010 RESULT ----- 22:46:31 --> \*\*\*PASS  
TEST 192020 HSIF REGISTER RESET CHECK  
TEST 192020 RESULT ----- 22:46:33 --> \*\*\*PASS  
TEST 192030 HSIF REGISTER SYSTEM RESET CHECK

TEST 192030 RESULT ----- 22:46:36 --> \*\*\*PASS  
TEST 192050 HSIF FLASH MEMORY CHECK  
TEST 192050 RESULT ----- 22:46:36 --> \*\*\*PASS  
TEST 192100 HSIF RELAY OFF LEAK CURRENT CHECK  
TEST 192100 RESULT ----- 22:46:46 --> \*\*\*PASS  
TEST 192110 HSIF DC RELAY CHECK  
TEST 192110 RESULT ----- 22:47:05 --> \*\*\*PASS  
TEST 192200 HSIF DC INIT ADJUSTMENT CHECK  
TEST 192200 RESULT ----- 22:47:13 --> \*\*\*PASS  
TEST 192210 HSIF DATA VD INIT ADJUSTMENT CHECK  
TEST 192210 RESULT ----- 22:49:52 --> \*\*\*PASS  
TEST 192220 HSIF JR PLL PRETUNE INIT ADJUSTMENT CHECK  
TEST 192220 RESULT ----- 22:50:02 --> \*\*\*PASS  
TEST 192230 HSIF MUX TIMING INIT ADJUSTMENT CHECK  
TEST 192230 RESULT ----- 22:50:40 --> \*\*\*PASS  
TEST 192240 HSIF DUTY INIT ADJUSTMENT CHECK  
TEST 192240 RESULT ----- 22:50:56 --> \*\*\*PASS  
TEST 192300 HSIF DR DC VOLTAGE & RON/ROF CHECK  
TEST 192300 RESULT ----- 22:51:26 --> \*\*\*PASS  
TEST 192310 HSIF DR OUTPUT CURRENT & IMPEDANCE CHECK  
TEST 192310 RESULT ----- 22:51:28 --> \*\*\*PASS  
TEST 192320 HSIF DIAG CP REFERENCE VOLTAGE CHECK  
TEST 192320 RESULT ----- 22:51:55 --> \*\*\*PASS  
TEST 192400 HSIF LIMITER FAIL SENSE CHECK  
TEST 192400 RESULT ----- 22:52:01 --> \*\*\*PASS  
TEST 192410 HSIF LIMITER FAIL/MASK OPERATION CHECK  
TEST 192410 RESULT ----- 22:52:02 --> \*\*\*PASS  
TEST 192800 HSIF PLL LOCK DETECT CHECK  
TEST 192800 RESULT ----- 22:52:02 --> \*\*\*PASS  
TEST 192810 HSIF JR PLL FREQUENCY CHECK  
TEST 192810 RESULT ----- 22:52:21 --> \*\*\*PASS  
TEST 192820 HSIF JI PLL FREQUENCY CHECK  
TEST 192820 RESULT ----- 22:52:40 --> \*\*\*PASS  
TEST 192830 HSIF TRIGGER OUTPUT CHECK  
TEST 192830 RESULT ----- 22:52:46 --> \*\*\*PASS  
TEST 192840 HSIF DDS CLK LOCK DETECT CHECK

TEST 192840 RESULT ----- 22:52:46 --> \*\*\*PASS  
TEST 192850 HSIF DDS SIGNAL FREQUENCY CHECK  
TEST 192850 RESULT ----- 22:53:51 --> \*\*\*PASS  
TEST 192860 HSIF DDS SIGNAL LEVEL CHECK  
TEST 192860 RESULT ----- 22:53:59 --> \*\*\*PASS  
TEST 192900 HSIF DATA VD LINEARITY CHECK  
TEST 192900 RESULT ----- 22:54:14 --> \*\*\*PASS  
TEST 192910 HSIF MUX FUNCTION CHECK  
TEST 192910 RESULT ----- 22:55:43 --> \*\*\*PASS  
TEST 192920 HSIF DR DUTY CHECK  
TEST 192920 RESULT ----- 22:55:46 --> \*\*\*PASS  
TEST 192930 HSIF DR FUNCTION CHECK  
TEST 192930 RESULT ----- 22:56:02 --> \*\*\*PASS  
TEST 192940 HSIF TIMING SHIFT CHECK  
TEST 192940 RESULT ----- 22:56:02 --> \*\*\*PASS  
\*           DIAGNOSIS           END           AT           2022/11/22           22:56:08  
\*  
SYSTEM RESULT .....>> \*\*\*PASS